

RHUMBA Project Concept

RHUMBA Concept

- Green Project Concept
- Normal Grade Chassis (21" 25" 29") → To increase Productivity & Value engineering
- Market : South America

RHUMBA benefits

- ◇ Proper Picture Quality for 21 inches normal TV (DNle Jr)

21" Picture



DNle Jr

Product

21" 25" 29" Analogue 50Hz (Chassis)

Market

South America

Launching

July 2005

Product Chassis

21" 25" 29" (KS7A → K16A)

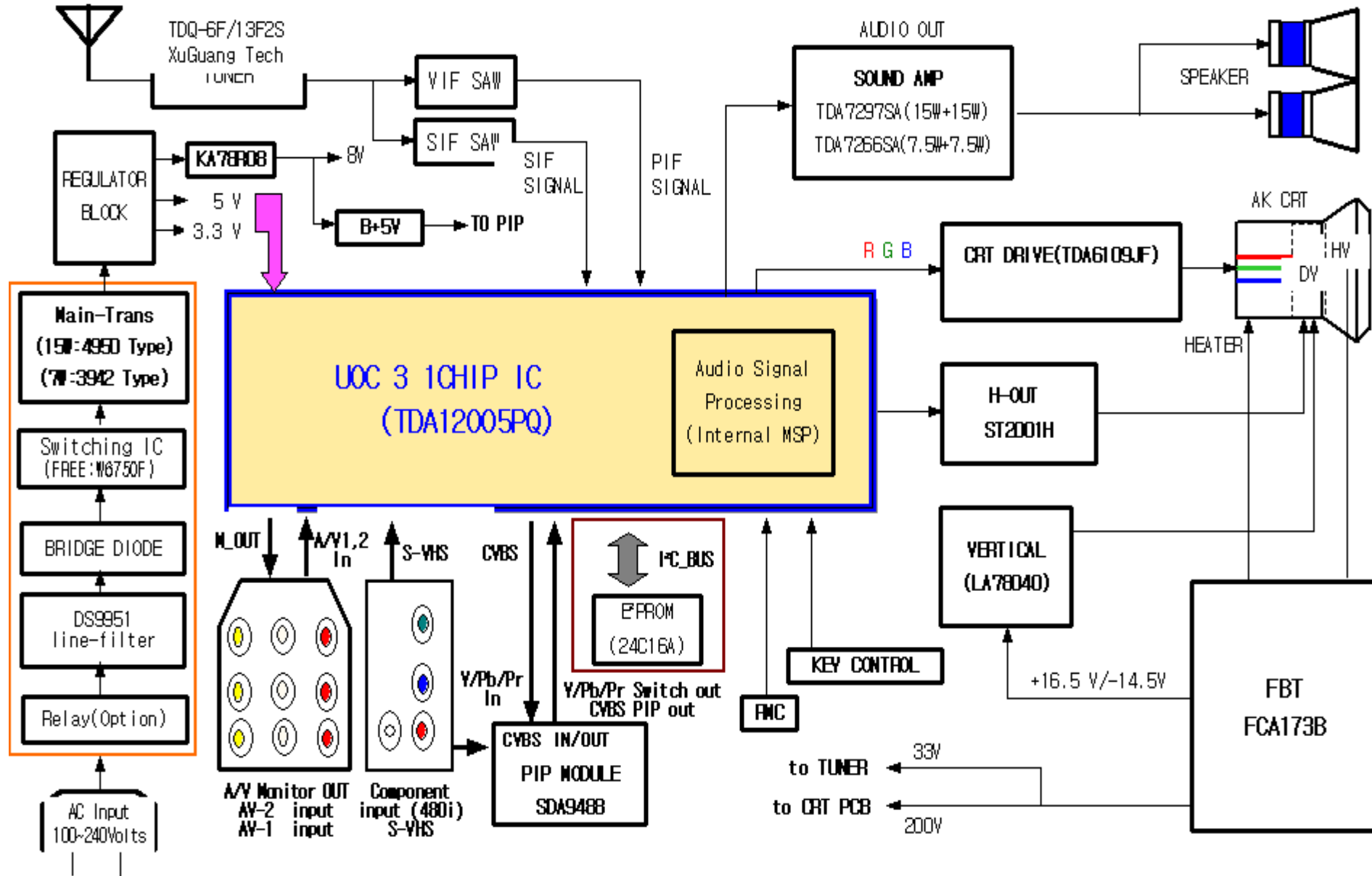
Benefits

DNle Jr

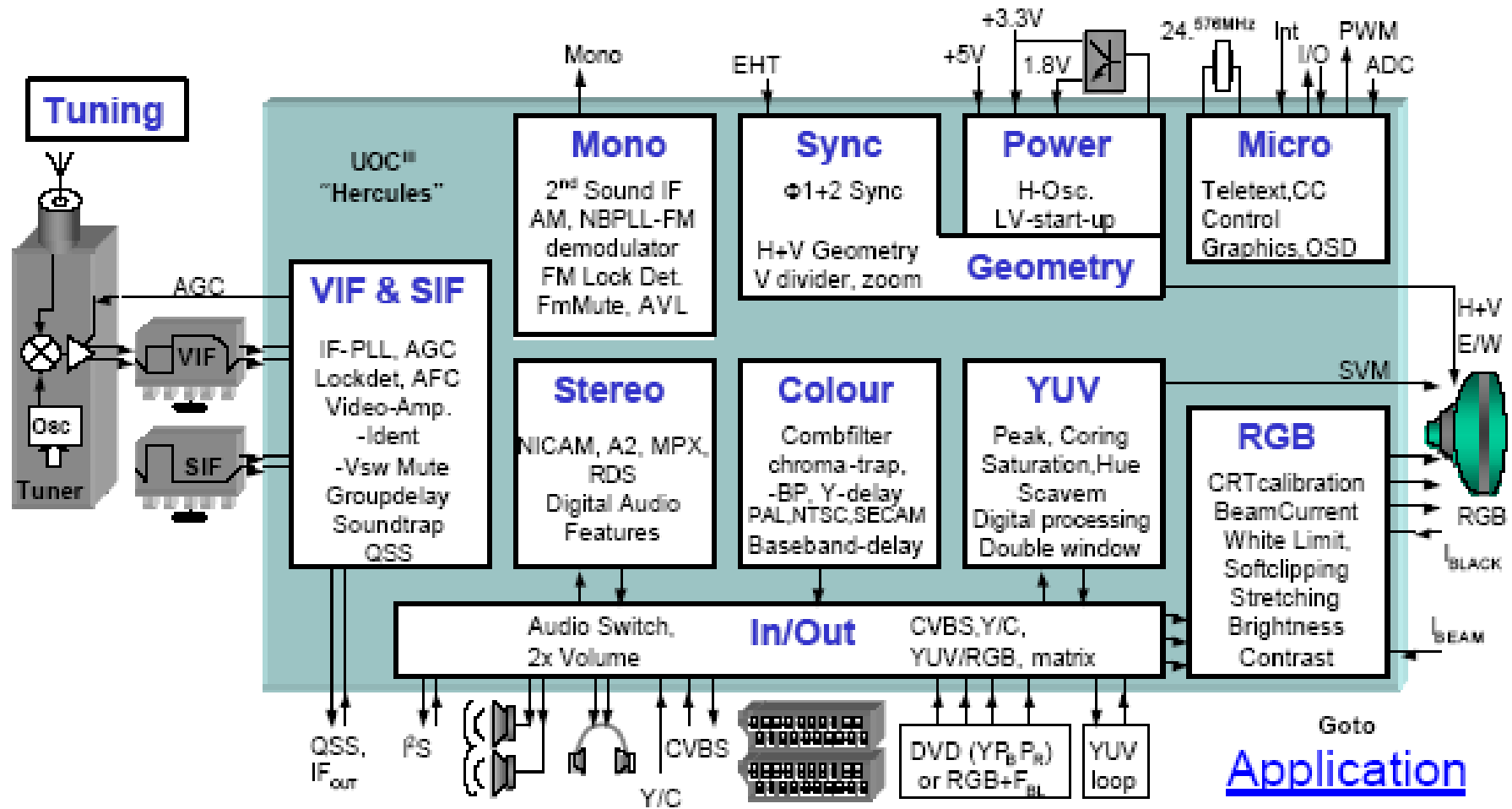
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21" SET Chassis \$10↓ (KS7A)

K16A Chassis Blocks Diagram



Functional blocks UOCIII



UOC3(TDA120XX) Pin Description

Pin No	Name	Register	Port Type	Initial	Description (Micom Pin 1 ~ 11, 54 ~ 64)
2	pIR	P0.5	Open Drain		- Remocon IR
4	pDcoil	P1.0	Push Pull		- Degaussing Coil
6	pPower	P1.3	Push Pull	0	- High : Power On - Low : Power Off
7	pSCL	P1.6	Push Pull	0	- I2C Bus Clock
8	pSDA	P1.7	Push Pull	0	- I2C Bus Data
10	pLED	P2.0	Push Pull	1	- Led (When Remocon is operated on Stand By Mode)
11	pSoundMute	P2.1	Push Pull	1	- High : Sound Mute On - Low : Sound Mute Off
12	BUS STOP	P3.0	Open Drain		-BUS STOP → Low, The other → High
13	X-RAY	P3.1	Open Drain		- X-Ray detect
14	pPanelKey ₂	P3.2	Open Drain		- Panel Key(Power switch key)
15	pPanelKey ₁	P3.3	Open Drain		-Panel Key 1 (Channel up, Channel Down, Volume Up, Volume Down, Menu)

Factory Data/Option1

Function Name	Description	Initial	Min	Max
1. System	CL > CP > CT-N	CL		
2. Video Mute	OFF > 100mS > 200msS > 300mS > 400mS > 500msS > 600mS > 700mS > 800msS > 900mS > 1000mS	400mS	OFF	1000mS
3. AV Jack	1RCA > 2RCA > 2RCA+S > 2RCA+DVD > 2RCA+S+DVD	2RCA+S+DVD	-	-
4. Sound	Line Stereo > Stereo > Virtual Dolby	Stereo	-	-
5. Volume Curve	Large > Small	Large	-	-
6. Initial Lang.	English > Spain > Portugal > France	English	-	-
7. Tilt	Off > On	Off	-	-
8. DNle Jr	Off > On	On		
9. PIP	Off > 1-Tuner > 2-Tuner	1-Tuner		
10. Auto Power On	Off > On	Off		
11. Caption	Off > On	On		
12. Vchip	Off > On	Off		
13. Child lock	Off > On	On		
14. Plug&play	On	On		
15. Standby Led	Off > On	Off		

Factory Data/Option2

Function Name	Description	Initial	Min	Max
1. X-Ray Protect	Off > On	Off		
2. HighDeviation	Off > On	Off		
3. V-Guard	Off > On	On		
4.ACS	Off > On	Off		
5.CRT	4:3 ZOOM / 4:3 ZOOM 16:9	4:3 ZOOM		
6. LNA	Off > On	Off		
7. Hotel Mode	Off > On	Off		
8.Philippines	Off > On	Off		

Factory Data / Deflection

Name (Function)	Description	Sub Add & Bit	Initial	Min	Max
V Amp	DAC setting Control 0 amplitude 80% 20 amplitude 100% 3F amplitude 120%	h10[0] ~ h10[5]	32	0	
V Shift	DAC setting Control 0 shift -5% 20 no correction 3F shift +5%	h12[0] ~ h12[5]	32	0	
H EW	DAC setting Control 0 output current 700 mA 3F output current 0 Ma	h0A[0] ~ h0A[5]	32	0	
H Shift	DAC setting Control 0 -2 ms 20 0 3F +2 ms	h05[0] ~ h05[5]	32	0	
V Linearity	DAC setting Control 0 ratio bottom/top of screen: 117% 20 no correction 3F ratio bottom/top of screen: 85%	h08[0] ~ h08[5]	32	0	
V S-Correction	DAC setting Control 0 correction -10% 0E no correction 3F correction 25%	h11[0] ~ h11[5]	32	0	
V Slope	DAC setting Control 0 correction -20% 20 no correction 3F correction +20%	h0F[0] ~ h0F[5]	25	0	

Factory Data/Deflection

Function	Description	Sub Add & Bit	Initial	Min	Max
V Scroll V Zoom H Parabola	DAC setting Control 0 picture shift -18% 20 no picture shift 3F picture shift +18%		32	0	
	DAC setting Control 0 amplitude 75% 19 amplitude 100% 3F amplitude 138%		35	0	
	DAC setting Control 0 output current +262 mA (+55%) 11 output current 0 Ma 3F output current -262 mA (-55%)		32	0	
Upper Corner	DAC setting Control 0 output current +262 mA (+55%) 11 output current 0 mA 3F output current -262 mA (-55%)		32	0	
Lower Corner			32	0	
H Trapezium	DAC setting Control 0 output current at top of screen 100 mA lower that at bottom 20 no correction 3F output current at top of screen 100 mA higher than at bottom		32	0	
Bow	DAC setting Control 0 screen top and bottom 1.0 ms delayed with respect to centre 20 no correction 3F screen top and bottom 1.0 ms advanced with respect to centre		32	0	
Angle			32	0	

Factory Data / Video Adjust 1

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
BLOR	R Cutoff	DAC setting Control 0 -100 mV (R/G), -50mV (U/V) 20 no offset 3F +100 mV (R/G), +50mV (U/V)	h17[0] ~ h17[5]	32	0	
BLOG	B Cutoff	DAC setting Control 0 -100 mV (R/G), -50mV (U/V) 20 no offset 3F +100 mV (R/G), +50mV (U/V)	h18[0] ~ h18[5]	32	0	
WPR	R Drive	setting Control 0 gain -3 dB 20 no correction 3F gain +3 db	h20[0] ~ h20[5]	32	0	
WPG	G Drive	setting Control 0 gain -3 dB 20 no correction 3F gain +3 db	h21[0] ~ h21[5]	32	0	
WPB	B Drive	setting Control 0 gain -3 dB 20 no correction 3F gain +3 db	h22[0] ~ h22[5]	32	0	
BRT	Sub Bright	DAC setting Control 0 correction -0.4 V 20 no correction 3F correction +0.4 V	1B[0] ~ 1B[5]	12	0	23
CON	Sub Contrast	DAC setting Control 0 RGB amplitude -14 dB 20 RGB amplitude nominal 3F RGB amplitude +6 Db	1D[0] ~ 1D[5]	12	0	

Factory Data / Video Adjust 1

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
SAT	PAL/SECAM Sub Color	DAC setting Control 0 colour off (-52 dB) 17 saturation nominal 3F saturation +300%	1C[0] ~ 1C[5]	12	0	3
	NTSC Sub Color	DAC setting Control 0 colour off (-52 dB) 17 saturation nominal 3F saturation +300%		14	0	23
	NTSC Sub Tint			12	0	23
	YUV Sub Tint			32	0	23
	AKB Option			0	0	1
PF0 PF1	Peaking CF0 & Delay Mode ※ width of pre-shoot or overshoot	PF1 PF0 Centre frequency DELAY(Peaking center frequency and delay) 0 0 2.7 MHz 190 ns 0 1 3.1 MHz 160 ns 1 0 3.5 MHz 143 ns 1 1 4.0 MHz 125 ns ※ Move to Others Item		1	0	3
	Sub Sharpness-RF			23	0	23

Factory Data / Video Adjust2

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
	Melody Volume			35	0	100
DAC	RF AGC	DAC setting Control 0 tuner take-over at IF input signal of 0.4 mV 3F tuner take-over at IF input signal of 80 Mv	h15[0] ~ h15[5]	21		
AGC0 AGC1	IF AGC Speed	AGC1 AGC0 AGC speed 0 0 0.7 'norm = 0 0 1 norm = 1 1 0 3'norm = 2 1 1 6'norm = 3	h30[1] h30[2]	1	0	3
SMD0 SMD1	VM Mode	SMD1 SMD0 Mode 0 0 off = 0 0 1 SVM on video = 1 1 0 SVM on teletext or OSD = 2 1 1 SVM on video or OSD (fast switching) = 3	h49[0] h49[1]	0	0	3
VMA0 VMA1	VM Gain	VMA1 VMA0 Setting 0 0 off = 0 0 1 0.75 VP-P = 1 1 0 1.05 VP-P = 2 1 1 1.50 VP-P = 3	h49[2] h49[3]	0	0	3
SVM0 SVM1 SVM2	VM Delay	SVM0 TO SVM2 Delay setting SVM2 SVM2 ' 100 ns + SVM1 SVM1 ' 50 ns + SVM0 SVM0 ' 25 ns	h48[0] h48[1] h48[2]	0	0	7

Factory Data/Video Adjust2

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
BLS	Blue Stretch	BLS Blue stretch mode 0 off 1 on	h45[1]	0	0	1
	G2 Adjust Bright			42	0	
SOc0 SOc1	Soft Clipping Level	SOc1 SOc0 Voltage difference between soft clipping and pwl 0 0 0% above PWL level = 0 0 1 5% above PWL level = 1 1 0 10% above PWL level = 2 1 1 soft clipping off = 3	h1A[4] h1A[5]	1	0	3
PWL	Peak White Limit	PWL DAC Mode 0 00 peak white limiting circuit not active 1 00 peak white limiting circuit active(0.40 VBL-WH) : : 1 0F peak white limiting circuit active(0.60 VBL-WH) CVBS/Y input signal at which the Peak White Limiting is activated (max contrast setting). Nominal input signal: 0.7 VBL-WH.		15	0	16

Factory Data/Video Adjust2

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
CL0 CL1 CL2 CL3	Cathode Drive Level	CL3 - CL0 Control 0 gain -3 Db 7 nominal value F gain +3 dB	h42[0] h42[1] h42[2] h42[3]	4	0	15
IF-off	IF Demodulator	DAC setting Control 0 negative correction 20 no correction 3F positive correction	h14[0] h14[5]	38	0	63
FFI	Fast Filter IF PLL	FFI Condition 0 normal time constant 1 increased time constant		0	0	1

Factory Data/Video Adjust3

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
	PIP Contrast			2		
	PIP Bright			2		
	PIP Tint			1		
	PIP Color			10		
	PIP YC Delay			12		
	PIP PAL V. Pos			1		
	PIP NTSC V. pos			1		
	PIP H. Pos			0		
	PIP R Cutoff			9		
	PIP G Cutoff			7		
	PIP B Cutoff			8		
	PIP R Drive			115		
	PIP G Drive			127		
	PIP B Drive			115		

Factory Data/Video Adjust4

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
IFP1	IF Preset Value 1	During "mix-down" of DVB signals with an external reference carrier (CMB2/CMB1/CMB0 = 1/0/0) the frequency of the oscillator can be defined by means of the settings of the "IF Preset Value" registers (subaddress 28H and 29H).	h28[0] ~ h28[0]	32	0	63
IFP2	IF Preset Value 2		h29[0]	32	0	63
EPVI	IF PLL Osc Preset Value	EPVI condition 0 normal operation 1 preset value is loaded	h28[6]	0		
PGR	Preset Gain R	setting CRT drive voltage 0 45 VP-P 40 90 VP-P 7F 180 VP-P	h23[0] ~ h23[6]	20	0	127
PGG	Preset Gain G	setting CRT drive voltage 0 45 VP-P 40 90 VP-P 7F 180 VP-P	h24[0] ~ h24[6]	20	0	127
PGB	Preset Gain B	setting CRT drive voltage 0 45 VP-P 40 90 VP-P 7F 180 VP-P	h25[0] ~ h25[6]	20	0	127
	Turbo Center Frequency			0		
DCXO	DCXO Caps/NICAM Center			64	0	
DCXO	DCXO Scaling Control Gain			5	0	7

Factory Data/Video Adjust5

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
VAI	System I output signal amplitude correction	VAI Mode 0 no correction 1 amplitude +12%	h31[4]	0	0	1
BPS	Bypass of chroma base-band delay line	BPS Delay line mode 0 active (Default "0") 1 bypassed (In case of 1 , Color problem will be occurred on the top of display on AV Mode.)	h3C[1]	0	0	1
FBC	Fixed beam current	FBC Mode 0 switch-off with blanked RGB outputs 1 switch-off with fixed beam current During switch-off the magnitude of the discharge current of the picture tube is controlled by the black current loop. Dependent on the setting of the OSO bit the vertical scan can be stopped in an overscan position during that time so that the discharge is not visible on the screen. The switch-off procedure is as follows : When the switch-off command is received the RGB outputs are blanked for a time of about 2 ms. If OSO = 1 the vertical scan is placed in an overscan position If OSO = 0 the vertical deflection will keep running during the switch-off time The soft-stop procedure is started by doubling the frequency of the horizontal output pulse The fixed beam current is forced via the black current loop The soft-stop time has a value of 43 ms, the fixed beam current is flowing during a time of 38 ms.	h41[1]	0	0	1
FBC1	Fixed beam current1	FBC1 Mode 0 fixed beam current is 1 Ma 1 fixed beam current is 2 mA	h4B[6]	0	0	1
IFS	IF Sensitivity	IFS IF sensitivity 0 normal 1 reduced	h31[3]	0	0	1
FCO	Forced Colour-On	FCO Condition 0 off 1 on	h3C[0]	0	0	1

Factory Data/Video Adjust5

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
DINT	Enable digital interface	DINT Mode 0 not active 1 active	h43[5]	0	0	1
SPT	Sync Performance Trick mode	SPT Mode 0 influence S/N detector on phi1 loop disabled 1 influence S/N detector on phi1 loop enabled	h36[5]	0	0	1
OSO	Switch-off in vertical overscan	OSO Mode 0 Switch-off undefined 1 Switch-off in vertical overscan	h3E[4]	0	0	1
CBS	Control sequence of beam current limiting	CBS Mode 0 normal operation (contrast → brightness) 1 control on contrast and brightness in parallel	h44[4]	0	0	1
CFA0 CFA1 CFA2	Comb filter modes	2 1 0 Comb filter 0 0 0 comb filter for PAL/NT modes with automatic control. Comb filter becomes active if IVWF = 1 and the CD output bits show one of the PAL/NTSC colour systems 0 1 0 comb filter active in forced NTSC-M mode (CM3-CM0 1111) on the condition that the output bits show (CD3-CD0) 0111. Software needed for VTR trick mode x x 1 comb filter forced off 1 x 0 comb filter "Forced on" for PAL-BG or NTSC-M; the IVWF bit must be 1	h39[4] h39[5] h39[6]	0	0	4
DL	Interlace	DL Status 0 interlace 1 de-interlace	h3E[1]	0	0	1
DTR	Chroma trap mode	DTR mode 0 single chroma trap 1 dual chroma trap, more suppression but less bandwidth	h3C[2]	0	0	1

Factory Data/Video Adjust5

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
OSVE	Black current measuring lines in overscan (for vertical zoom setting <1)	OSVE mode 0 normal operation 1 measuring lines in overscan	h40[6]	0	0	1
HCO	EHT Tracking	HCO Tracking mode 0 EHT tracking only on vertical 1 EHT tracking on vertical and EW ※ These functions are only available when the East-West drive output is active(AVLE=0).	h40[0]	?	0	1
Remark	1. CFA2 / CFA1 / CFA0 : if DNle Jr is Off, Video Adjust5 is set CFA0 without any relation of Comb Filter values. 2. In case that DL is TTX or MIX Mode, it is set 1 without any relation of Video Adjust 5 De Interlace values.					

Factory Data/YC Delay

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
	PAL Delay			8		
	NTSC Delay			8		
	PAL AV Delay			8		
	NTSC AV Delay			8		

Factory Data/Others

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
SBL	Service Blanking	SBL Service blanking mode 0 off 1 on	h40[3]	0	0	1
SLG0 SLG1	High Current Level	SLG1 SLG0 Mode 0 0 current level 220 mA = 0 0 1 current level 150 mA = 1 1 0 current level 280 mA = 2 1 1 current level 190 mA = 3	h42[5] h46[3]	1	0	3
LLB	Black Area	LLB Condition (After 0311 "0" FIX, Delete ITEM) 0 : internal bias current of BCL pin switched off 1 : internal bias current of BCL pin of 0.5mA switched on	h46[1]	2	0	1
BKS BSD	Black Stretch	BKS BSD Black stretch 0 0 off = 0 1 0 15 IRE = 1 1 1 30 IRE = 2	h45[7] h45[6]	2	0	2
?	OSD Brightness	?		25	0	31
PWL	PWL Active	PWL Mode (Merge to Peak White Limit of Video Adjust 2) 0 peak white limiting circuit not active 1 peak white limiting circuit active	h42[2]	1	0	1

Factory Data/Others

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
BPD	Bypass Peaking Delay	BPD Mode 0 normal operation 1 YUV peaking delay lines bypassed	h47[7]	0	0	1
RPA0 RPA1	Ratio Pre & After Shoot	RPA1 RPA0 Ratio 0 0 1 : 1 = 0 0 1 1.5 : 1 = 1 1 0 2 : 1 = 2	h47[4] h47[5]	2	0	2
RPO0 RPO1	Ratio posi & Nega Peaks	RPO1 RPO0 ratio 0 0 1 : 1 = 0 0 1 1 : 1.3 = 1 1 0 1 : 1.7 = 2 1 1 1 : 0.7 = 3	h47[2] h47[3]	1	0	3
DSK DSA	Dynamic Skin Control Dynamic skin tone angle	DSA DSK Condition 0 0 off = 0 0 1 117 = 1 1 1 123 = 2	h45[4] h46[0]	1	0	2
WS0 WS1	Gamma control and white stretch settings	GAM WS1 WS0 Expansion [1] APL [2] 0 0 0 0% - = 0 1 0 1 6% 17% = 1 1 1 0 8% 25% = 2 1 1 1 12% 28% = 3 [1] This figure indicates the maximum increase of the gain in the lower part of the characteristic (slope of the curve, see Fig. 74). [2] The APL (Average Picture Level) figure indicates the average luminance level at which the white stretch characteristic starts shifting from maximum stretching to the linear curve. At an increase of the APL of about 13% the curve is linear (see also Fig. 75).	h45[2] h45[3] h44[7]		0	3

Name	Function	Description	Sub Add & Bit	Initial	Min	Max
COR0 COR1	Video dependent coring (peaking)	COR1 COR0 Setting 0 0 off = 0 0 1 coring active between 0 and 20 IRE = 1 1 0 coring active between 0 and 40 IRE = 2 1 1 coring active between 0 and 100 IRE = 3	h47[1] h47[0]	0	0	3
CHSE0 CHSE1	PAL/NTSC Ident Sensitivity ※ PAL/NTSC ident sensitivity (burst amplitude at strong signal (typical value)	CHSE1 CHSE0 SENSITIVITY 0 0 -34 dB = 0 0 1 -37 dB = 1 1 0 -41 dB = 2 1 1 -46 dB = 3	h3C[4] h3C[5]	3	0	3
CLF	Comb Filter Diode Clamp	CLF Condition 0 clamp slow 1 clamp 7 times faster	h36[7]	1	0	1
TFR	DC Transfer Ratio	TFR Transfer ratio 0 no black level shift due to video content 1 black level shift 10 IRE for a white picture DC transfer Ratio of Luminance signal When this function is activated (TFR = 1) the black level of the RGB output signals is dependent on the average picture information. For a 'black' picture the black level is unaffected and the maximum black level shift for a complete 'white' picture (100 IRE) is 10 IRE in the direction 'black'. The black level shift is linearly dependent on the picture content.	h44[6]	1	0	1

Pin configuration of "Face-down" QIP versions

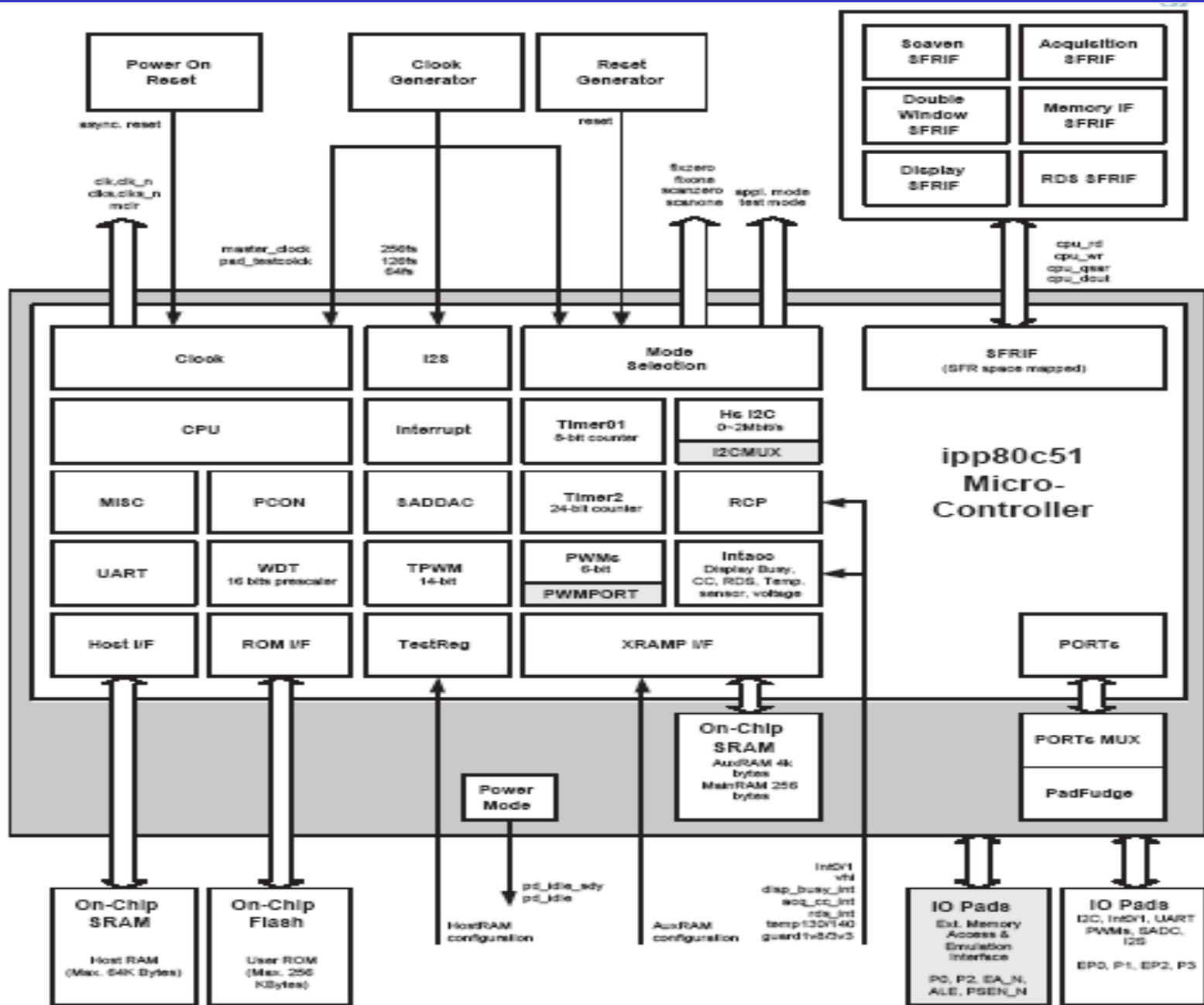
SSIF/REFIN/REFO	VP2	44	SV0I/FV0I/CVBSI	49
AGC2SIF/SW0/AVL	44	44	AUDIOIN4L/P2.2/PWM1	47
VCC8V	44	44	AUDIOIN4R/P2.3/PWM2	48
DVBOI/FV0I/FMRO	42	42	CVBS4	49
SIFAGC/DVAGC	41	41	AUDIOIN2L/P0.2	50
PLLIF	40	40	AUDIOIN2R/P0.0	51
GND2	39	39	CVBS2/Y2	52
AUDOUTSR	38	38	AUDIOIN3L/P1.4/RX/P2.4/PWM3	53
AUDOUTSL	37	37	AUDIOIN3R/P1.5/TX/P2.5/PWM4	54
AMOUT/OSSO/AUDEEM	36	36	CVBS3/Y3	55
AGCOUT	35	35	C2/3	56
DVBI/N2/SIFIN2	34	34	AUDOUTLTL	57
DVBI/N1/SIFIN1	33	33	AUDOUTLSR	58
GNDIF	32	32	AUDOUTHPL	59
IREF	31	31	AUDOUTHPR	60
VSC	30	30	CVBS0/PIP	61
VIFIN2	29	29	VSScomb	62
VIFIN1	28	28	VDDcomb	63
DECBG	27	27	DECSDM	64
SECPIL	26	26	YSYNC	65
GND1	25	25	YOUT	66
PH1LF	24	24	INSSW3	67
PH2LF	23	23	R/P_RIN3	68
VP1	22	22	GYIN3	69
DECDIG	21	21	B/P_BIN3	70
VSSA1	20	20	SYM	71
XTALOUT	19	19	FBISO/CSY	72
XTALIN	18	18	HOUT	73
GND3	17	17	EHTO	74
VDDA3(3.3V)	16	16	AV/LEWD	75
P3.3/ADC3	15	15	VDRA	76
P3.2/ADC2	14	14	VDRB	77
P3.1/ADC1	13	13	VGUARD/SWIO	78
P3.0/ADC0	12	12	GND3	79
P2.1/PWM0/P0.1	11	11	VP3	80
P2.0/TPMW/P0.4	10	10	BCLIN	81
VDDP(3.3V)	9	9	BLKIN	82
P1.7/SDA	8	8	RO	83
P1.6/SCL	7	7	GO	84
P1.3/T1	6	6	BO	85
P1.1/T0	5	5	VDDA1(3.3V)	86
P1.0/INT1	4	4	GND41	87
VDDC(1.8)/RESET	3	3	VDDA2(3.3V)	88
P0.5/INT0/P1.2/INT2	2	2	VREFAD	89
VSSC	1	1	VDDA(1.8V)	90

QIP90 Face-down version

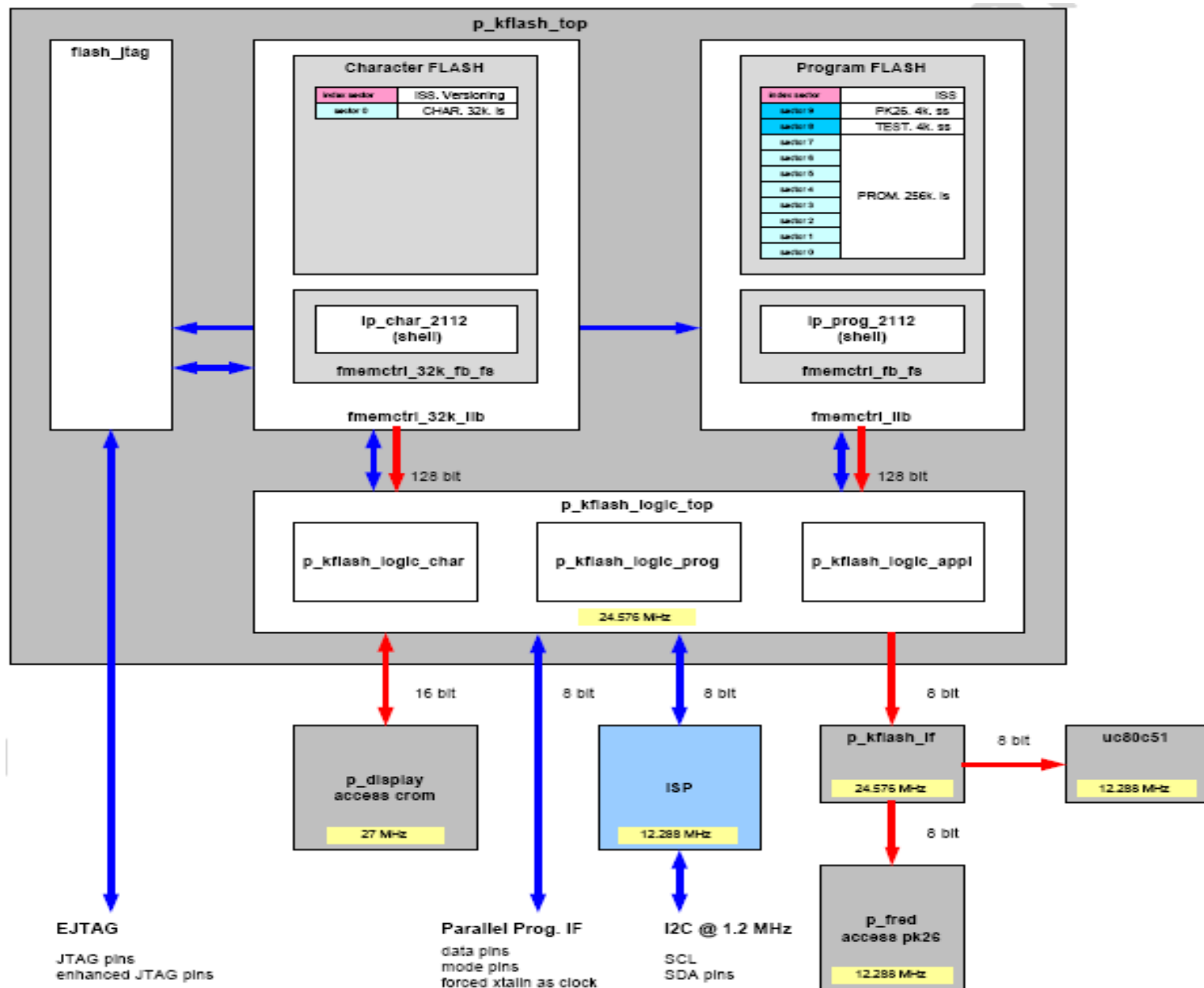
Control System Features

- ▶ 80C51 micro-controller core standard instruction set and timing
- ▶ 0.4883 ms machine cycle (6 clock cycles with 12.288 MHz derived from an xtal frequency of 24.576MHz)
- ▶ maximum 256k x 8-bit program ROM
- ▶ maximum of 8k x 8-bit auxiliary RAM
- ▶ auxiliary RAM page pointer
- ▶ 12-level interrupt controller for individual enable/disable with two level priority
- ▶ stand-by, idle and power-down modes
- ▶ watchdog timer
- ▶ two 16-bit timer/counters
- ▶ additional 24-bit timer (16-bit timer with 8-bit Pre-scaler)
- ▶ 16-bit data pointer
- ▶ five 6-bit pulse width modulator (PWM) outputs for control of TV analogue signals.
- ▶ one 14-bit PWM for voltage synthesis tuning control.
- ▶ 8-bit ADC with 4 multiplexed inputs.
- ▶ remote control pre-processor (RCP).
- ▶ I2C byte level bus interface.
- ▶ universal asynchronous receiver transmitter (UART)
- ▶ 24 General I/O.

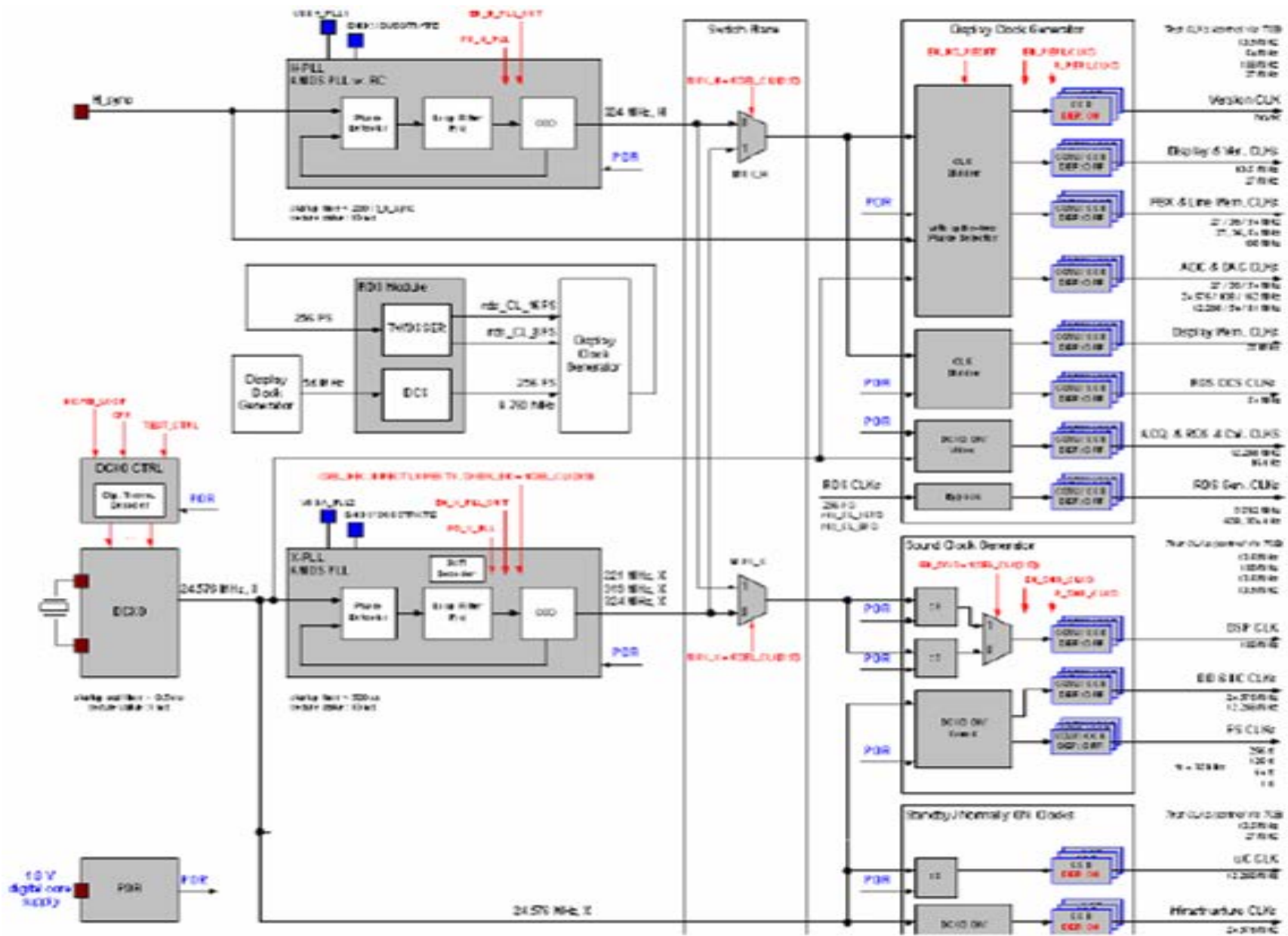
80C51 Microcontroller Block Diagram



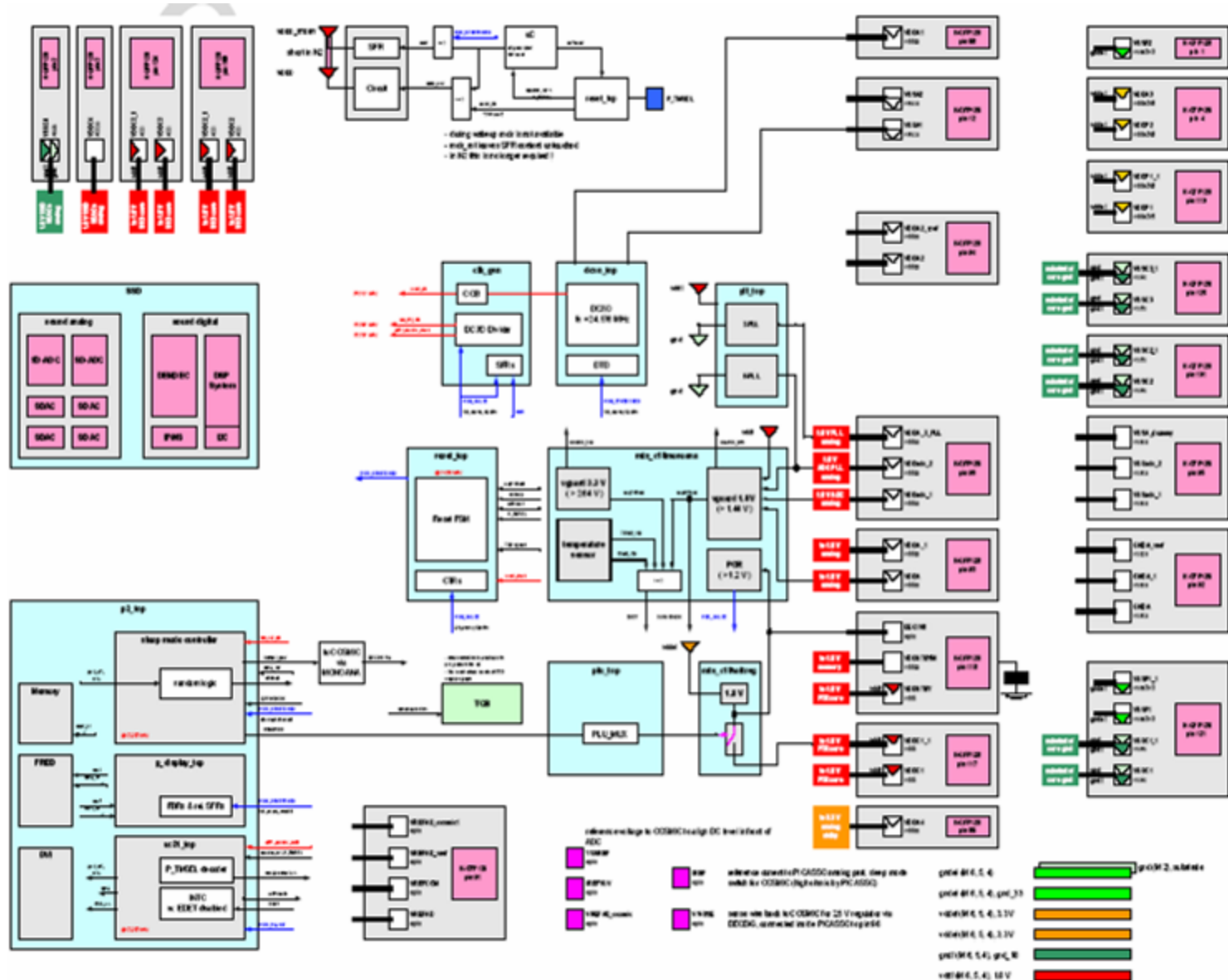
Flash Memory Block and Access Diagram



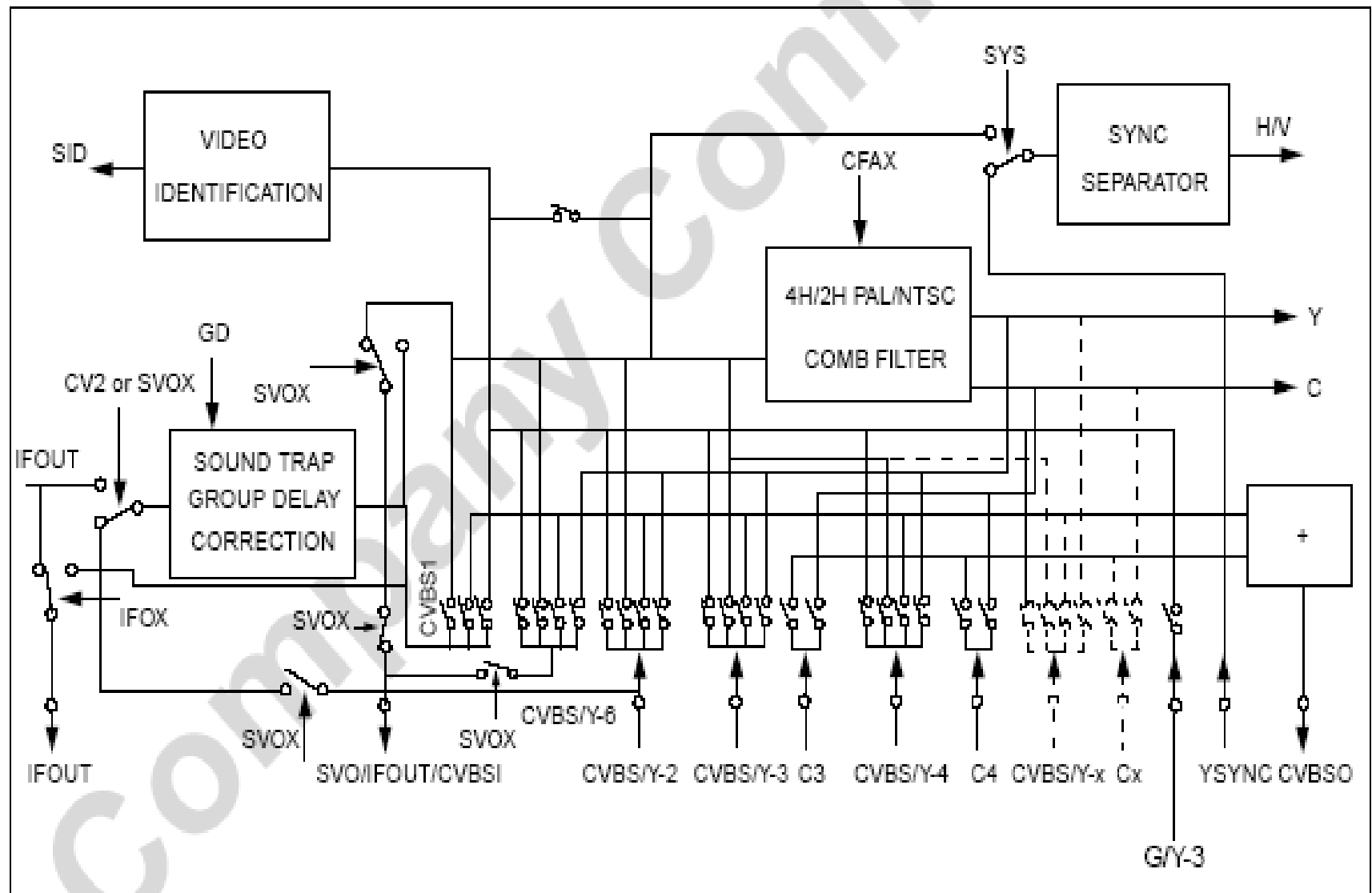
TCG m-Controller Clock System Diagram



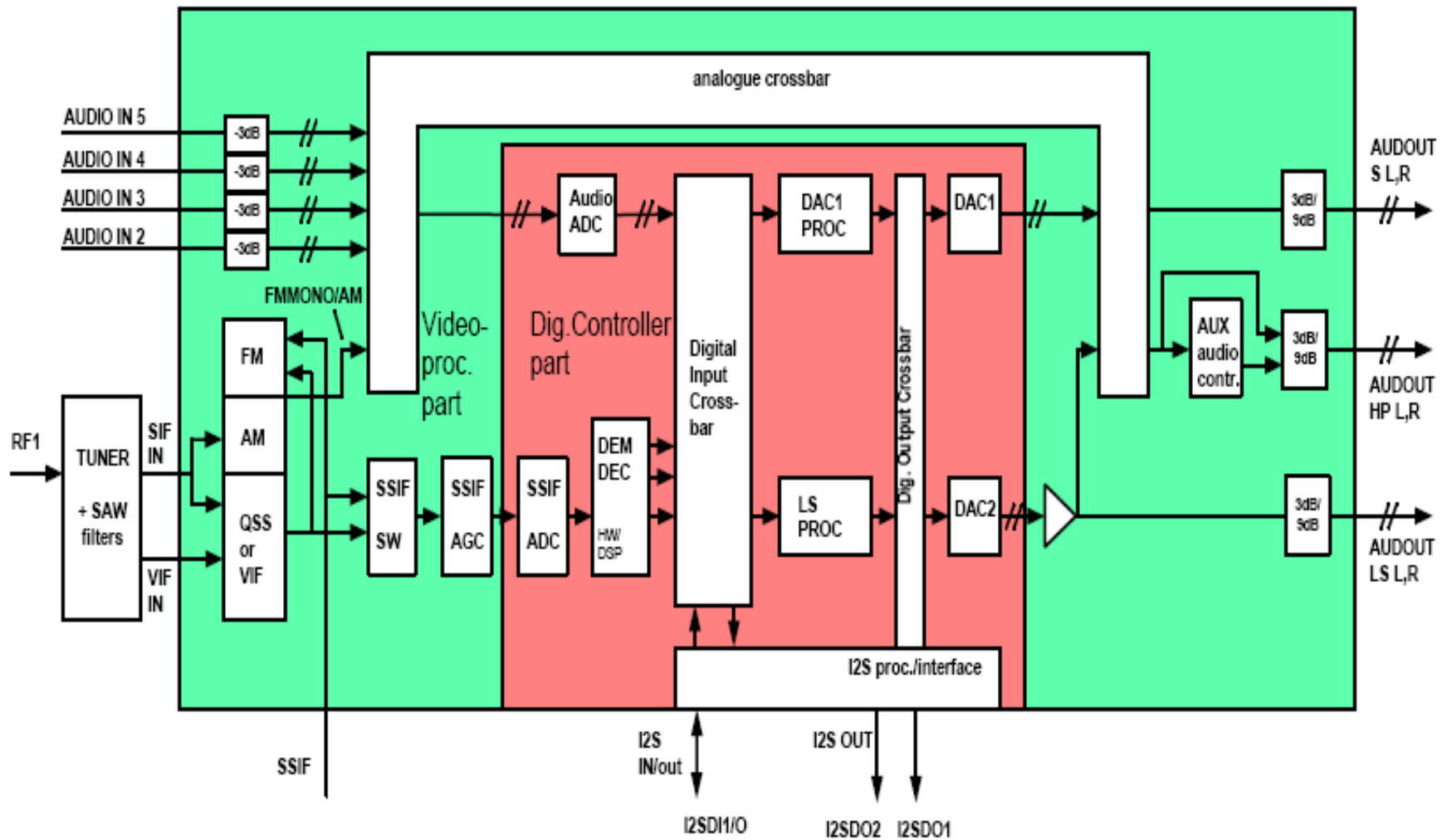
Supply Scheme with Voltage Guards and Power On Reset Unit



CVBS switch

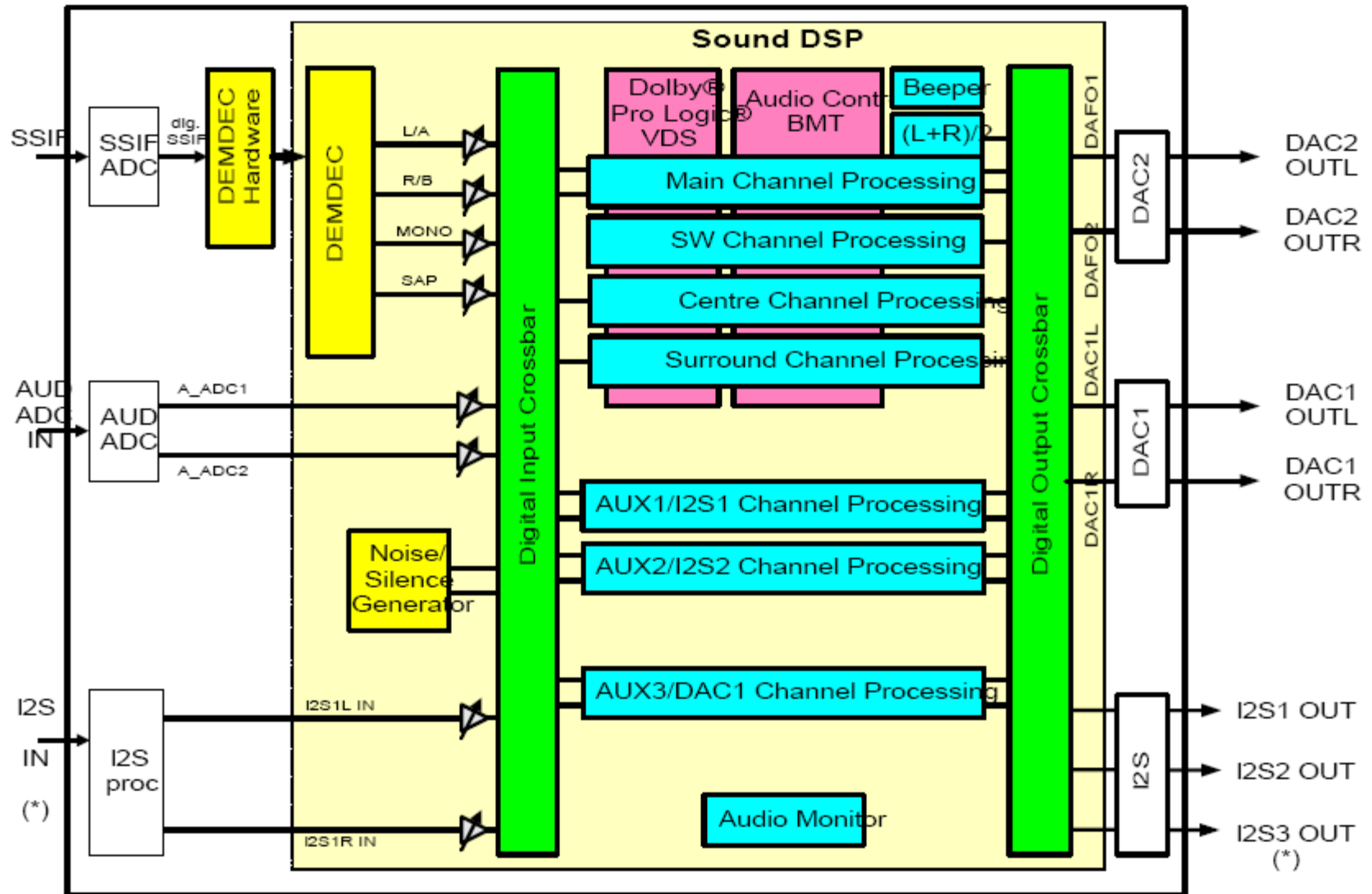


The UOCIII TV Sound Concept



(only relevant blocks, functions and signal flow for sound are shown)

Overview of the UOCIII sound functions on the digital controller



(*): connected to one pin that can be used alternatively as I2S IN or I2S3 OUT

Overview of the UOCIII sound functions on the digital controller

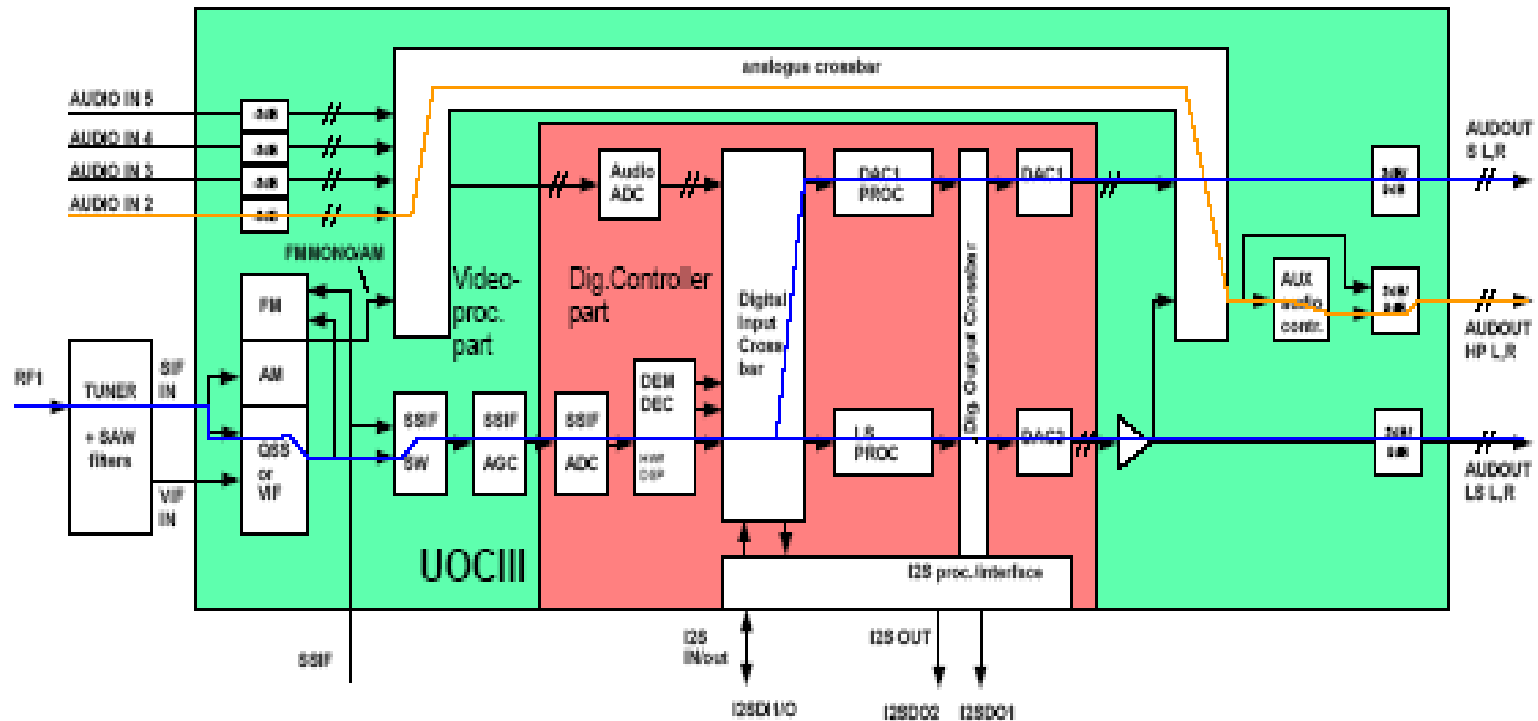
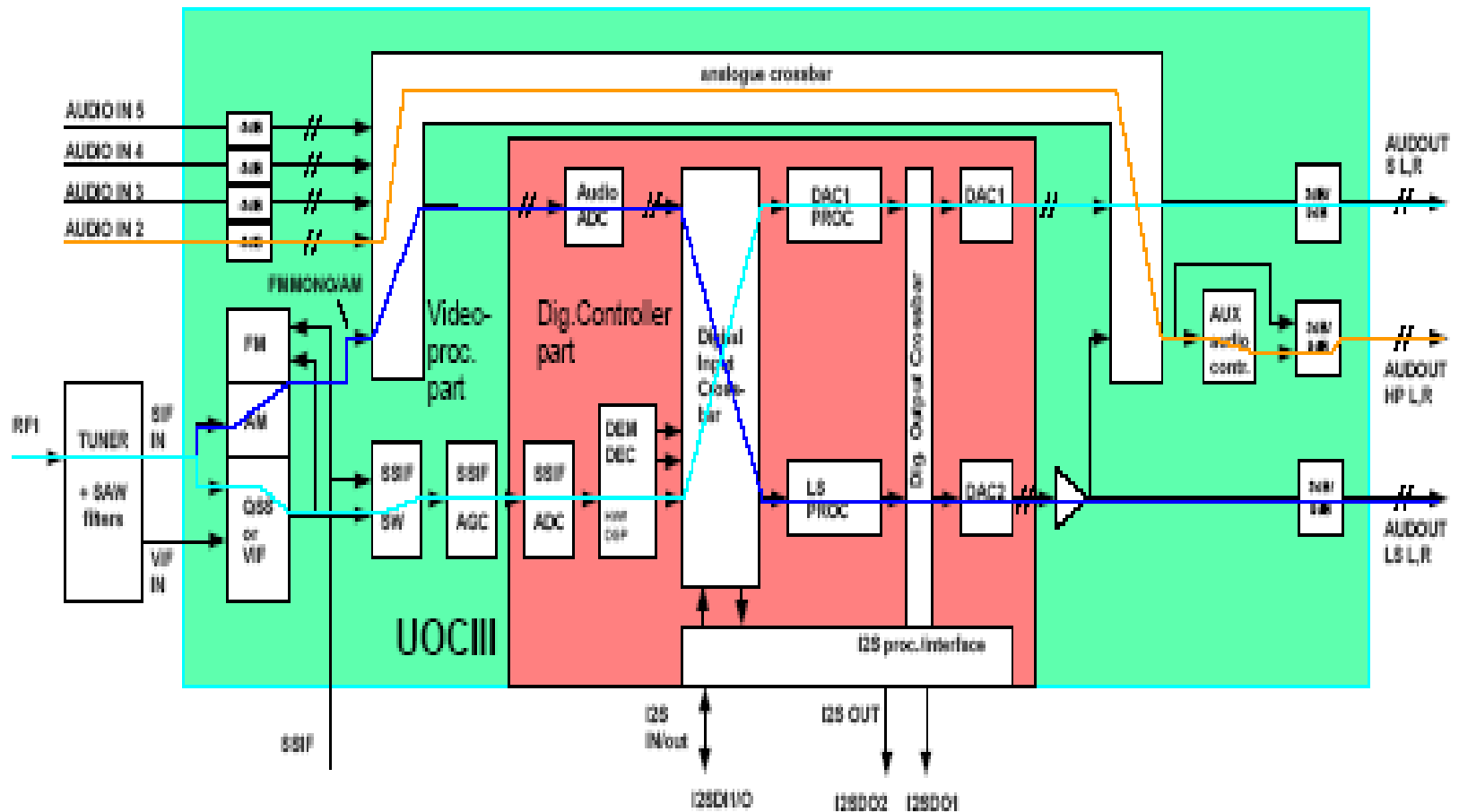


Figure 7 FM A2 and FM/NICAM use cases

Overview of the UOCIII sound functions on the digital controller



Overview of the UOCIII sound functions on the digital controller

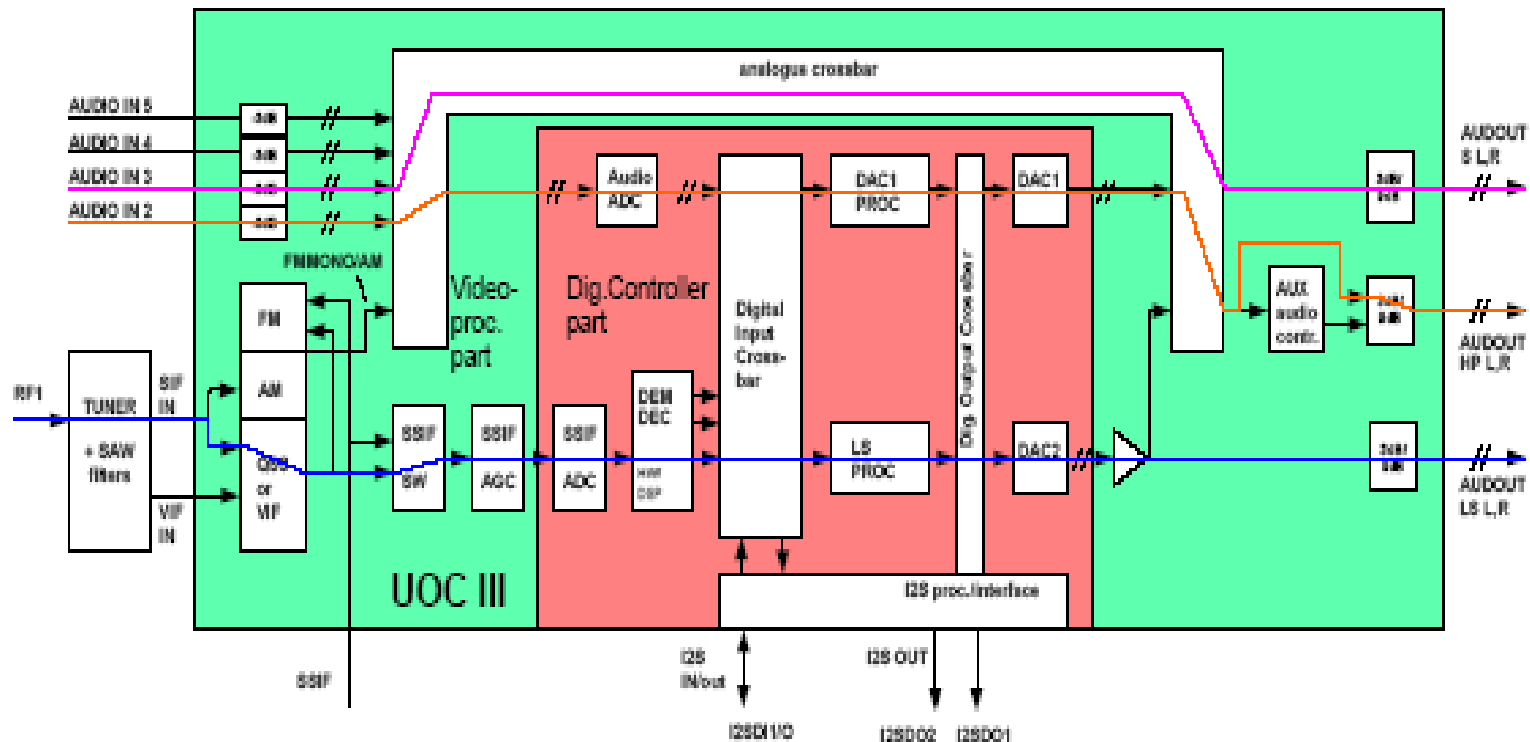
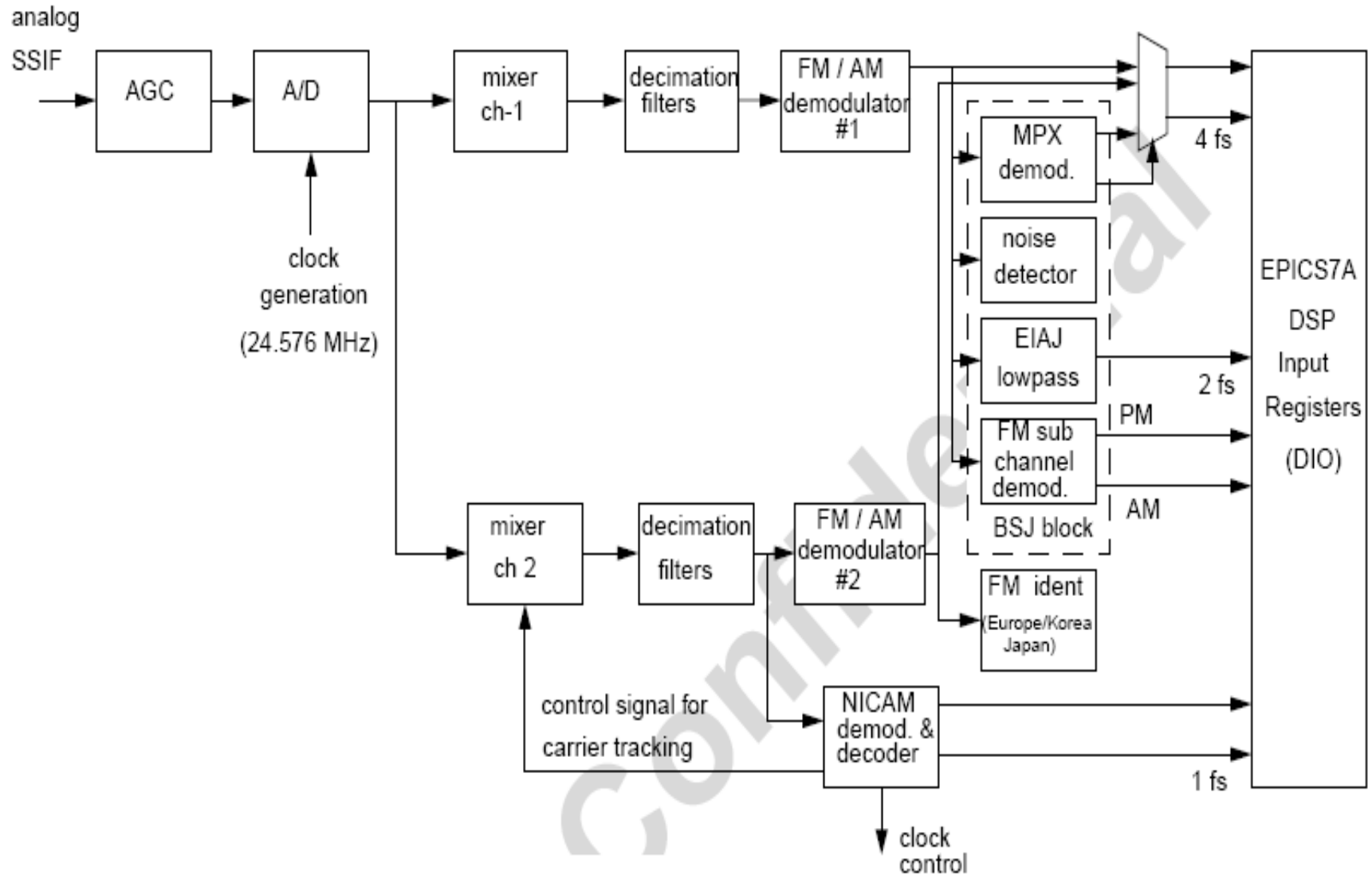
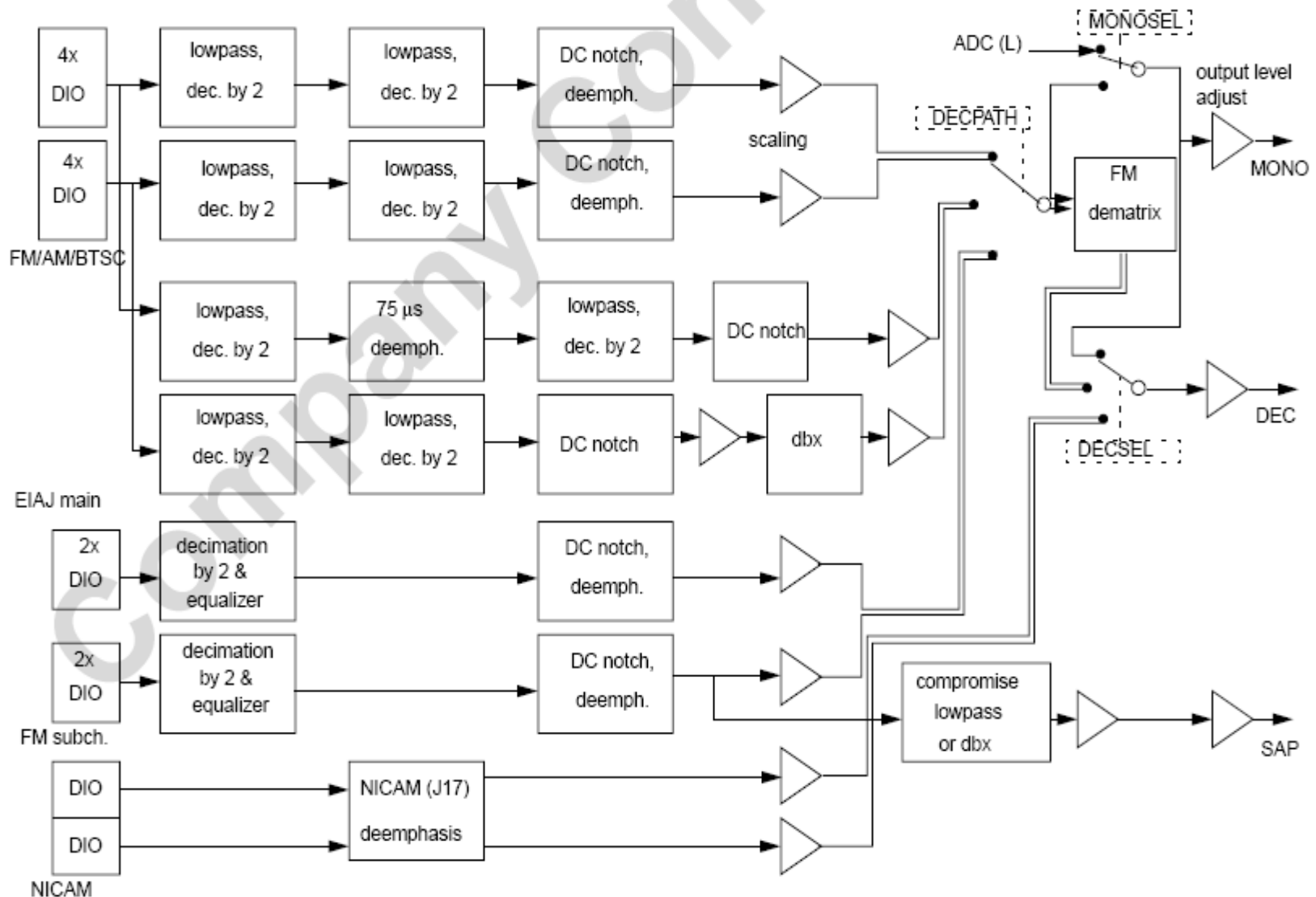


Figure 9 BTSC sound processing with independent headphone processing

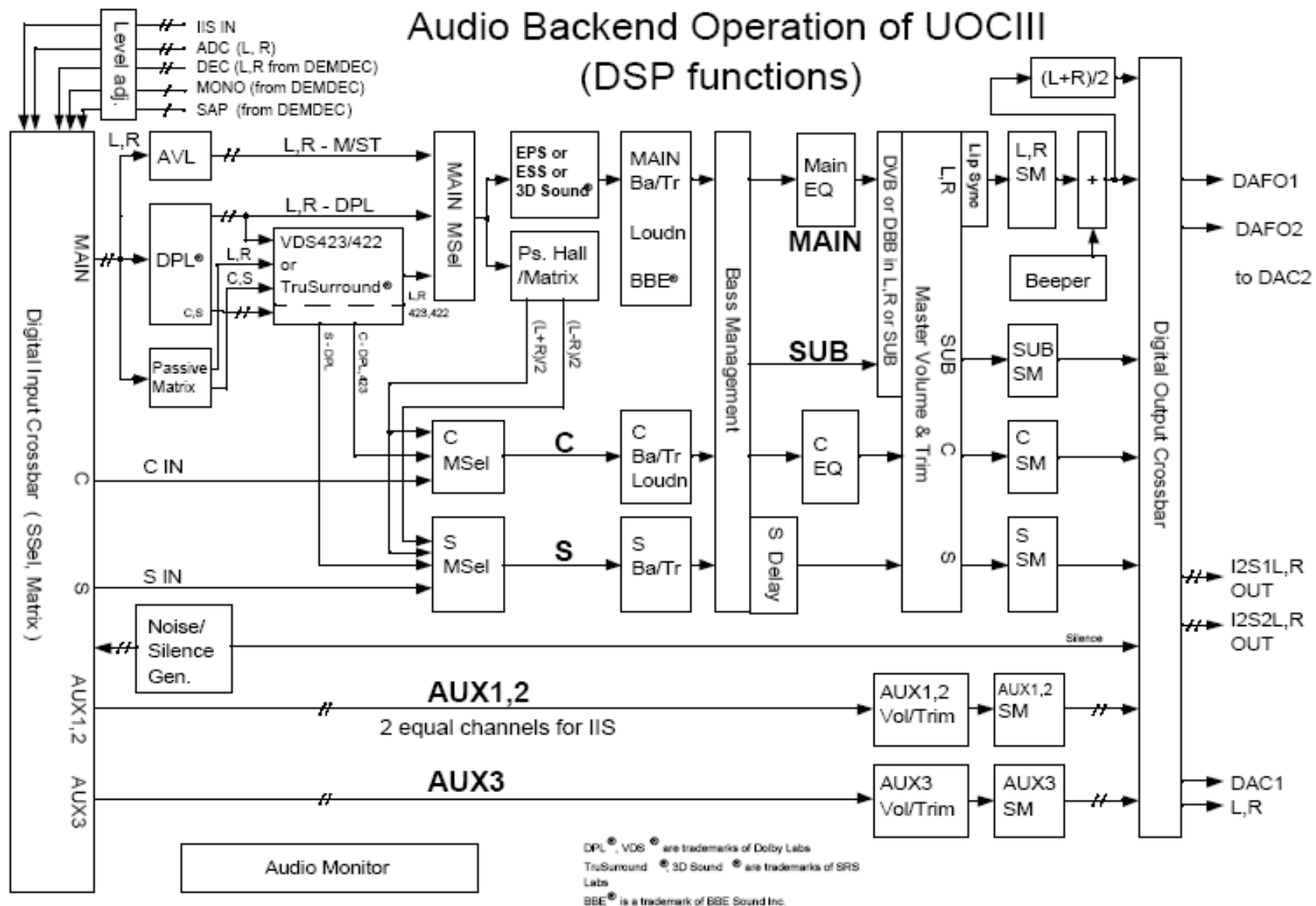
Demodulator and Decoder Block Diagram



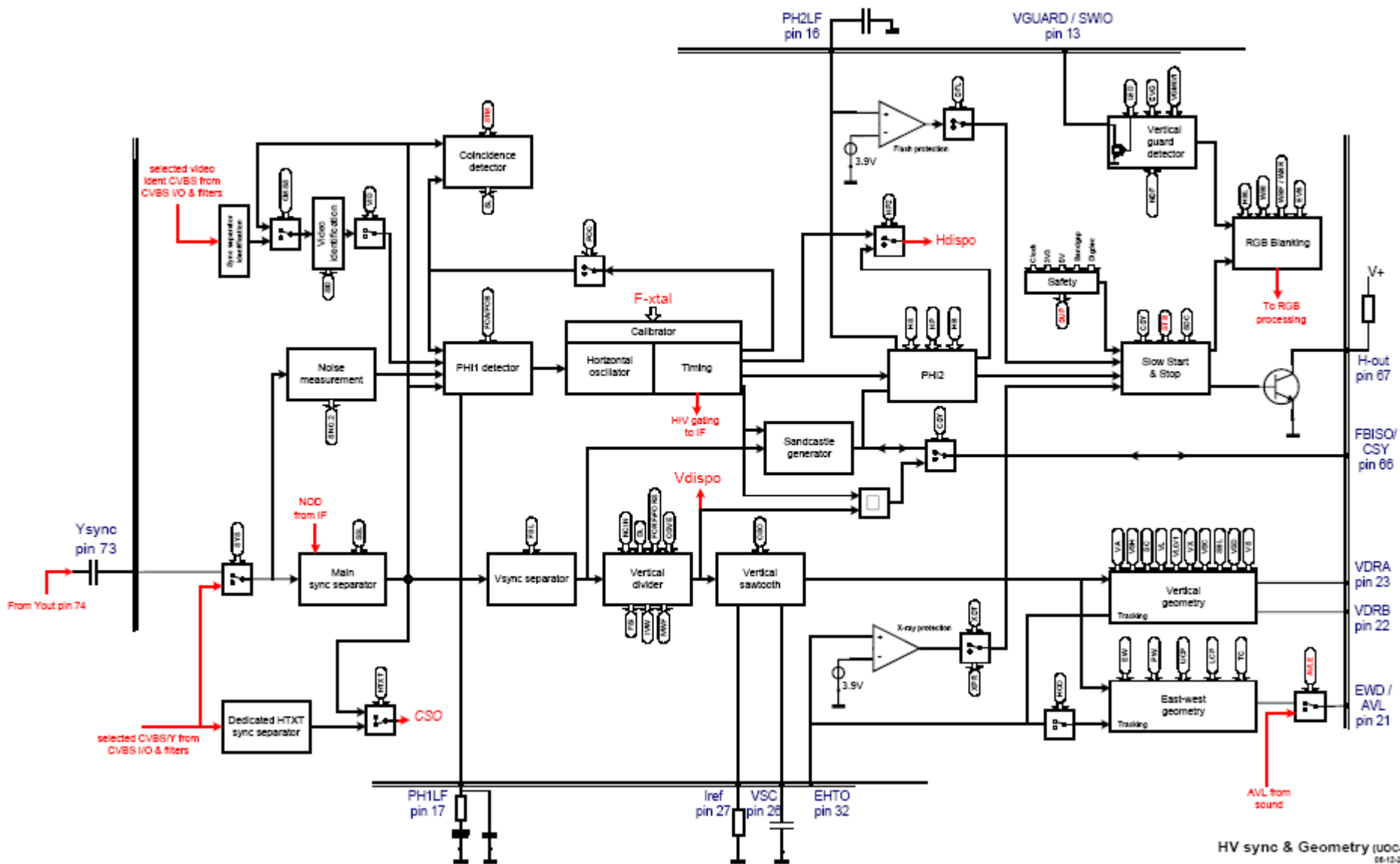
Signal processing modules



Audio Backend Operation of UOCIII

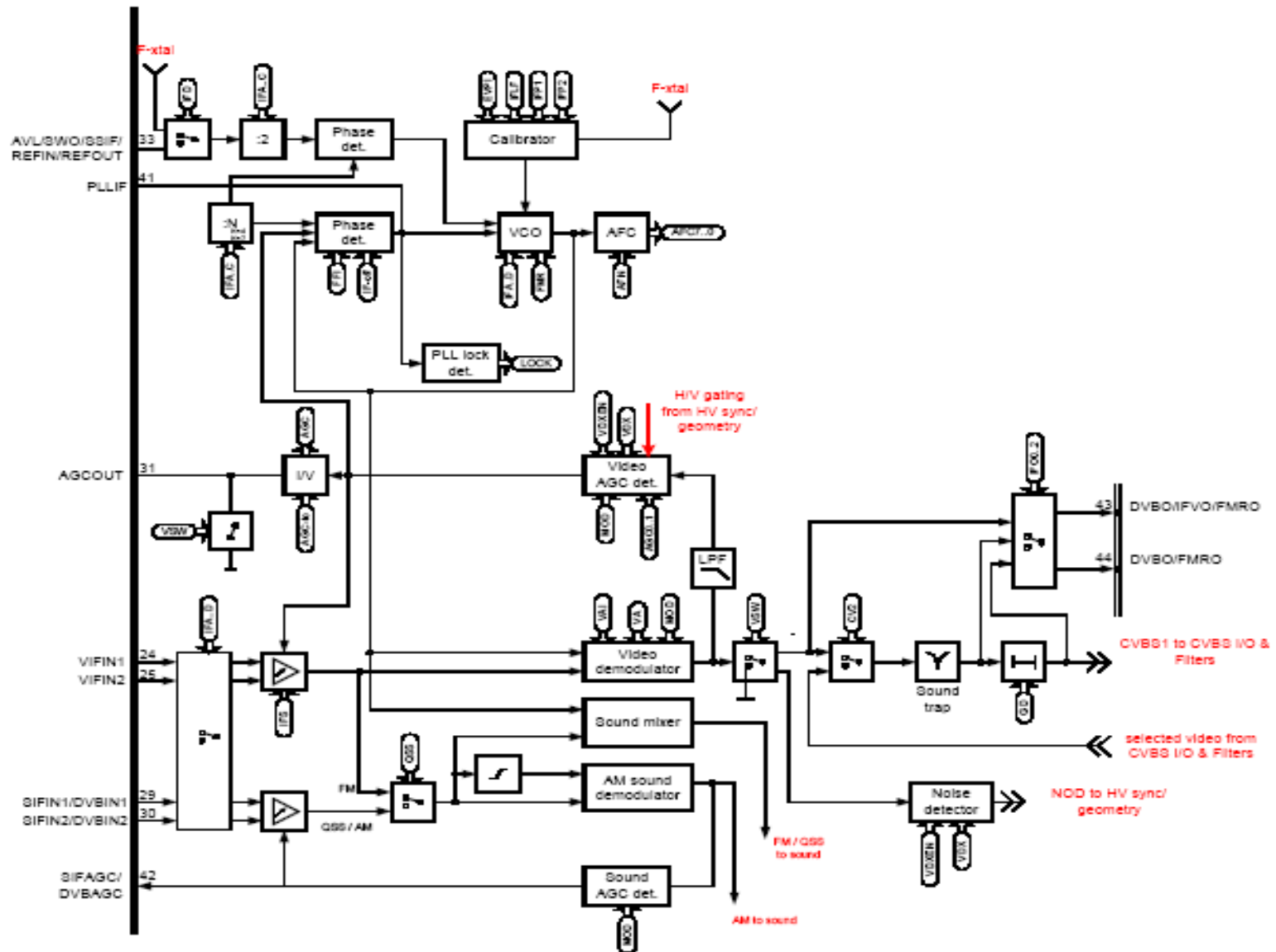


Syunc & Geometry block diagram

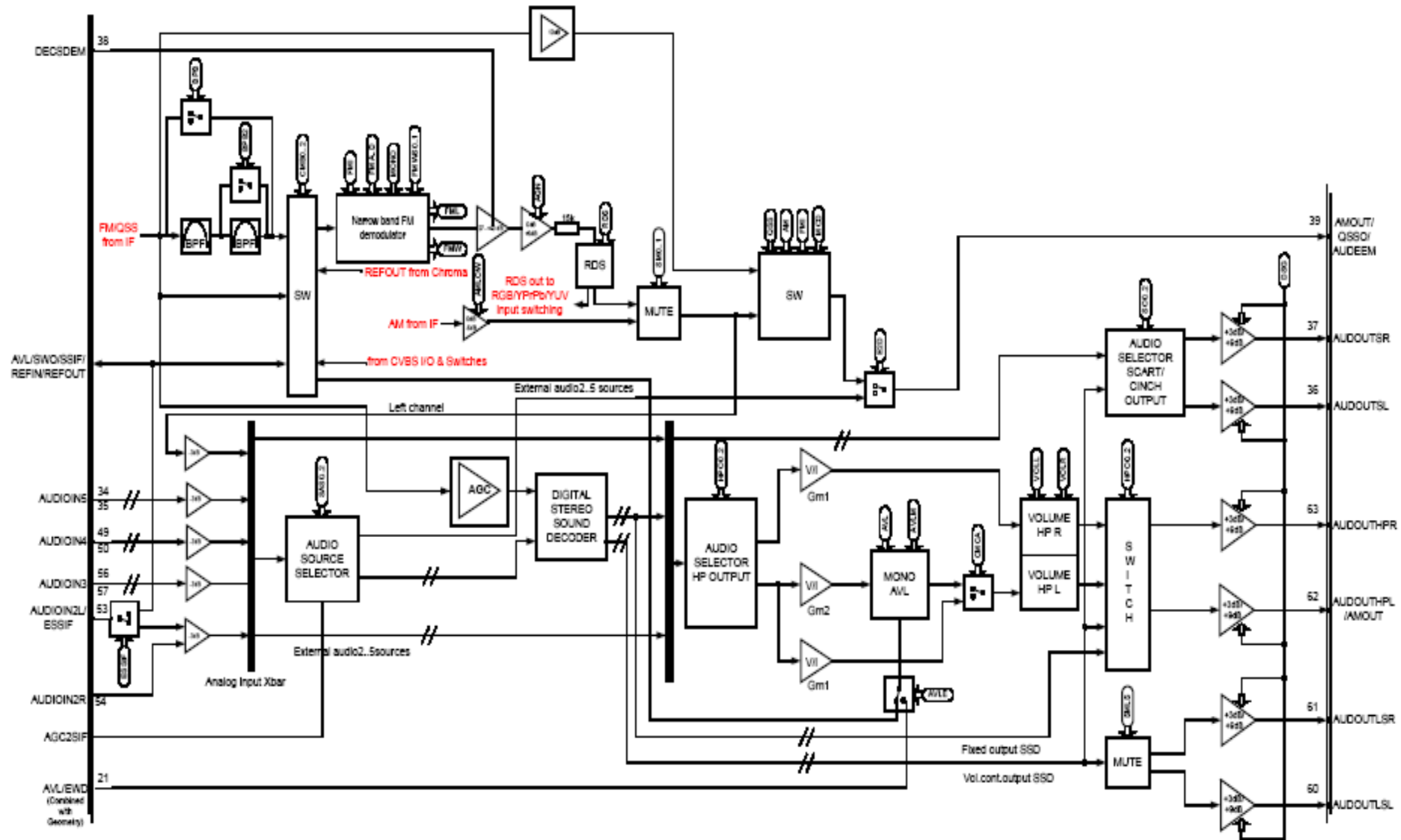


HV sync & Geometry (uoc-iii)
06-12-2002

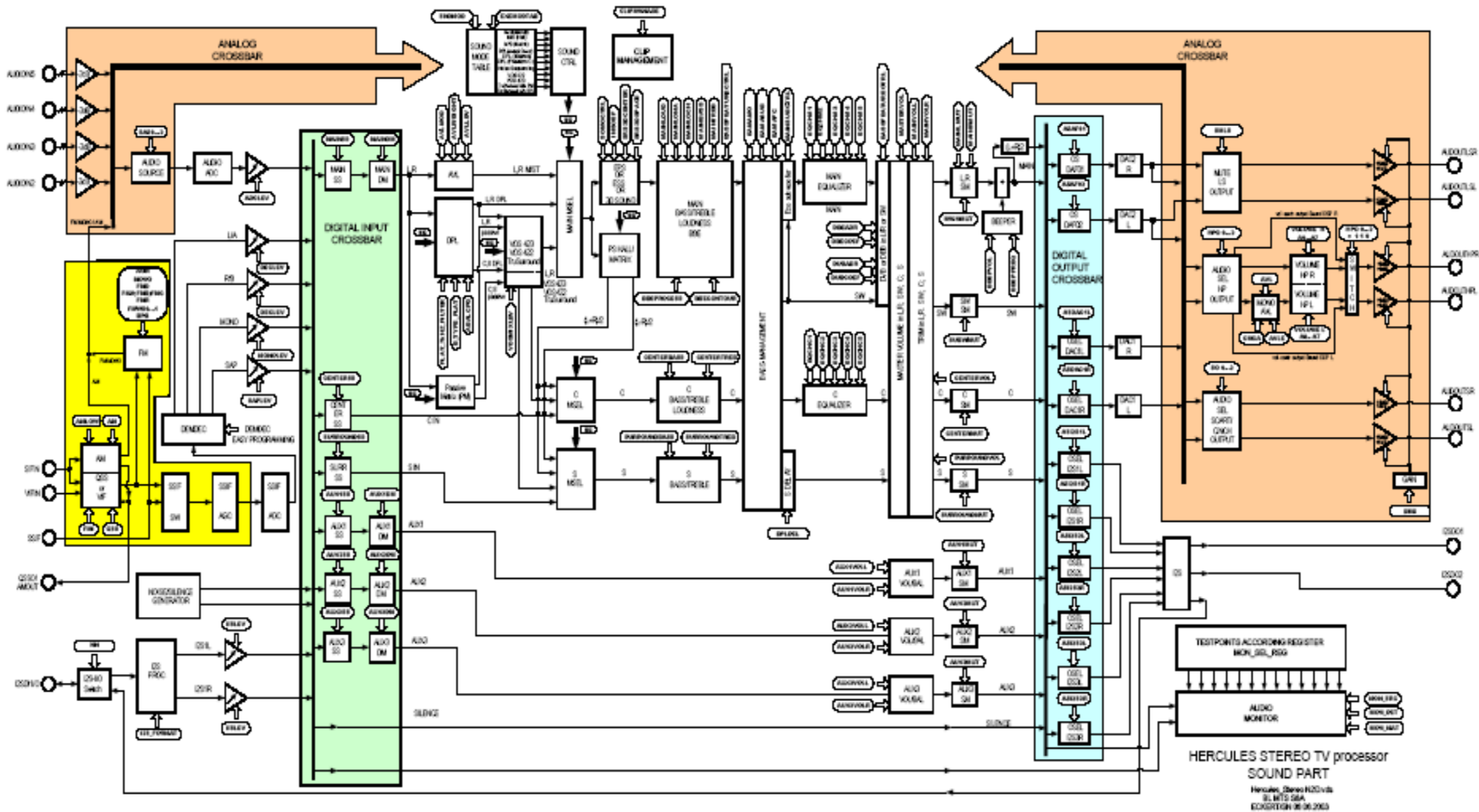
IF block diagram



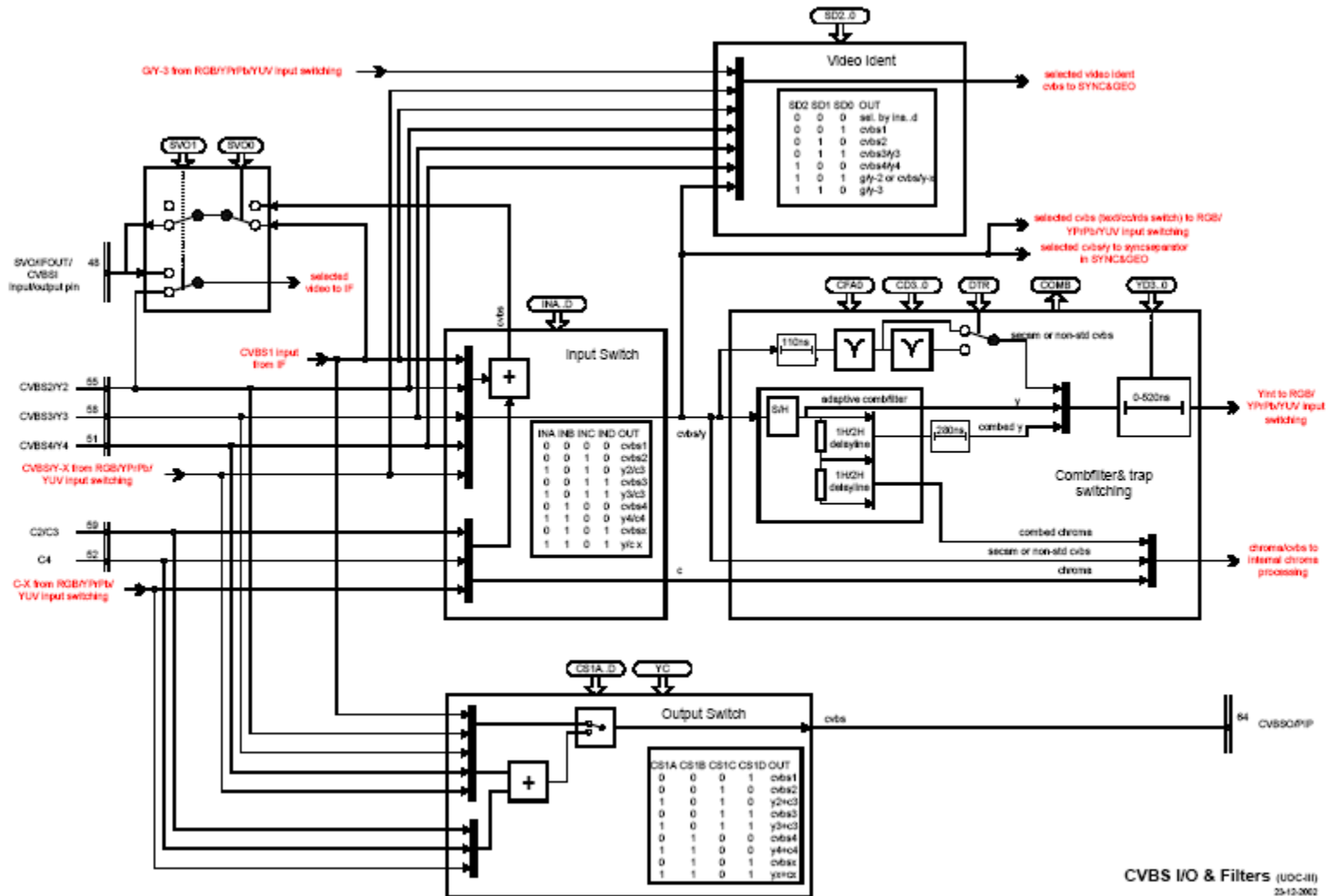
Analogue sound block diagram



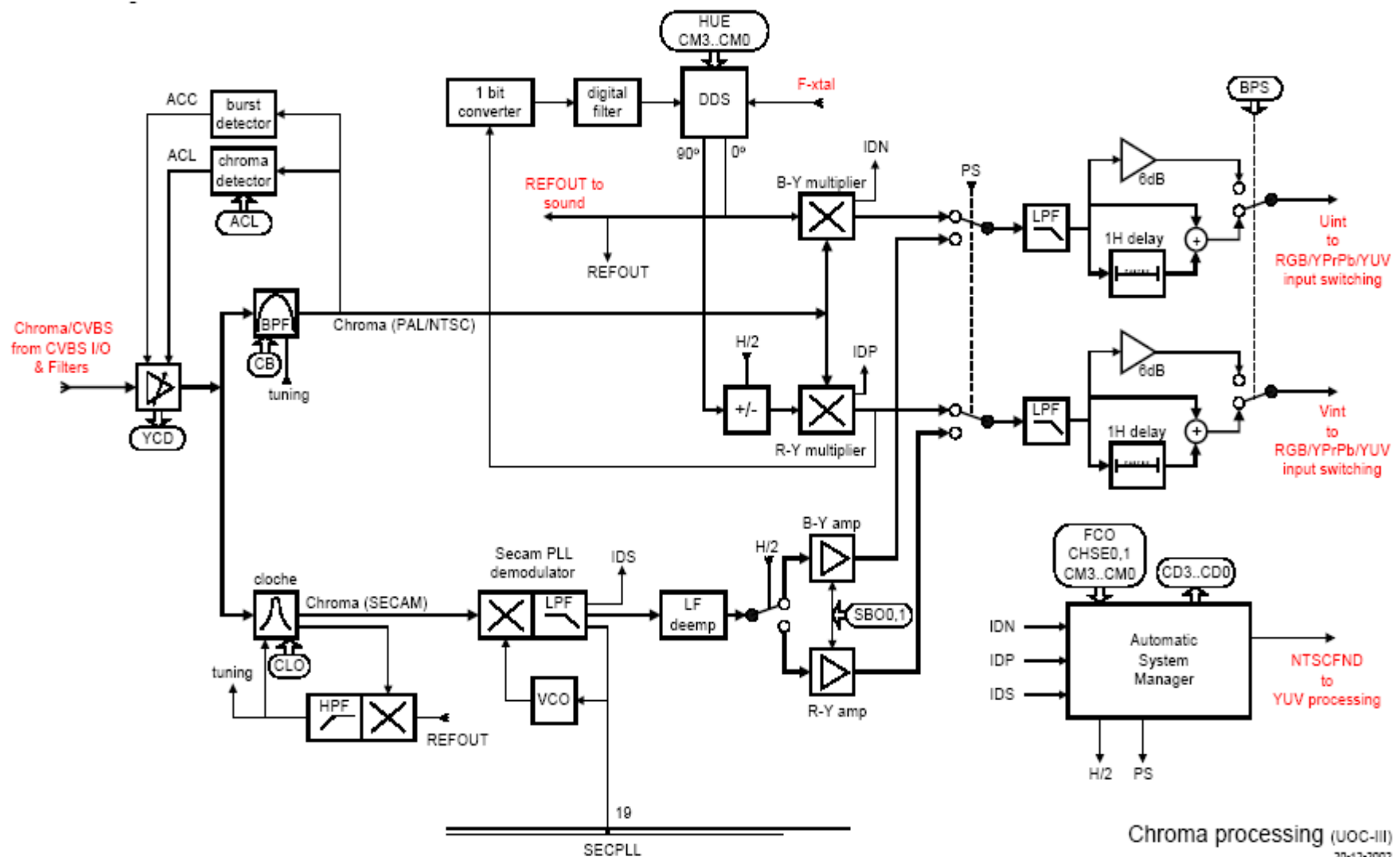
Block diagram stereo sound processor



CVBS I/O & Filters block diagram



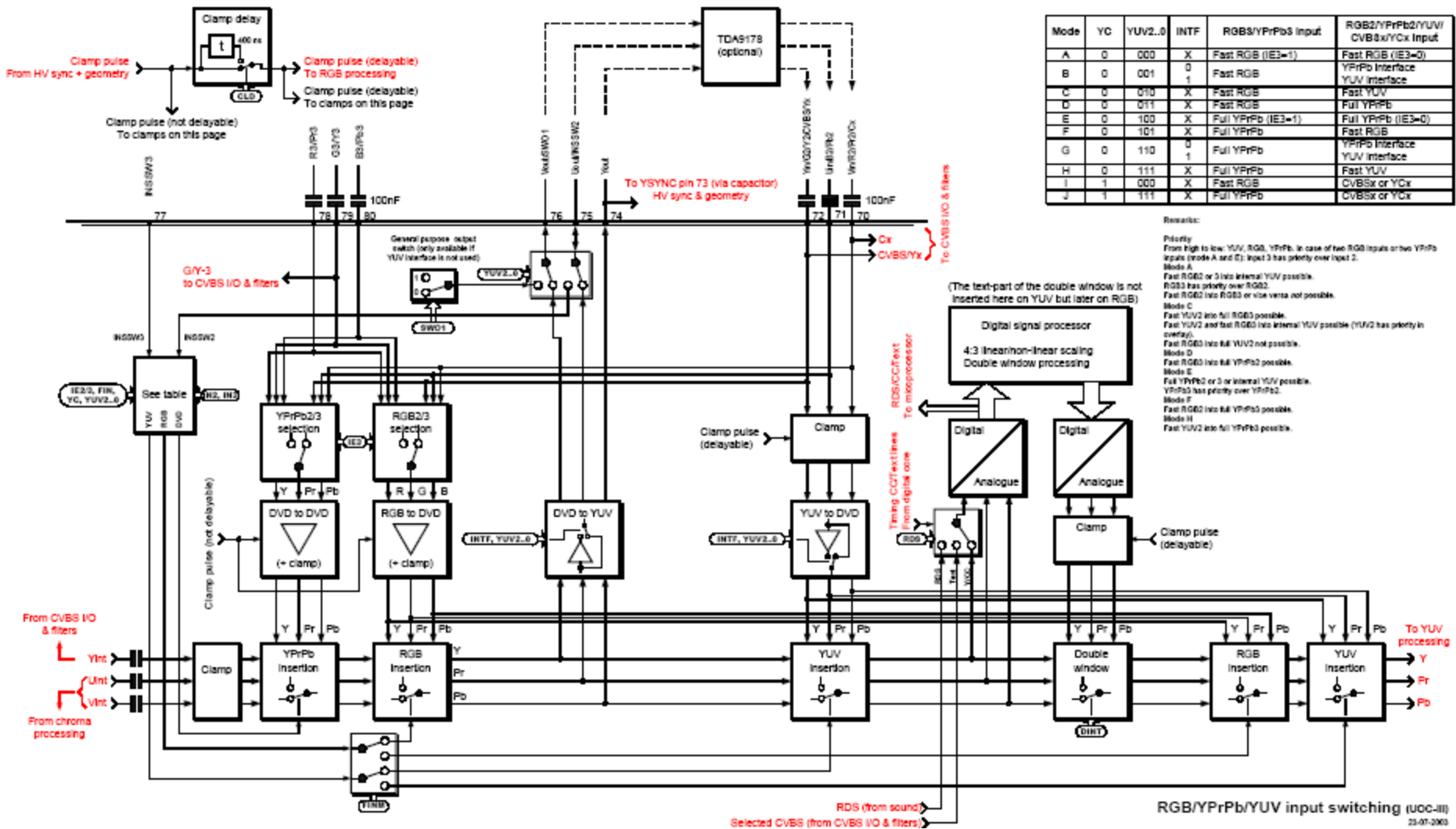
Chroma processing block diagram



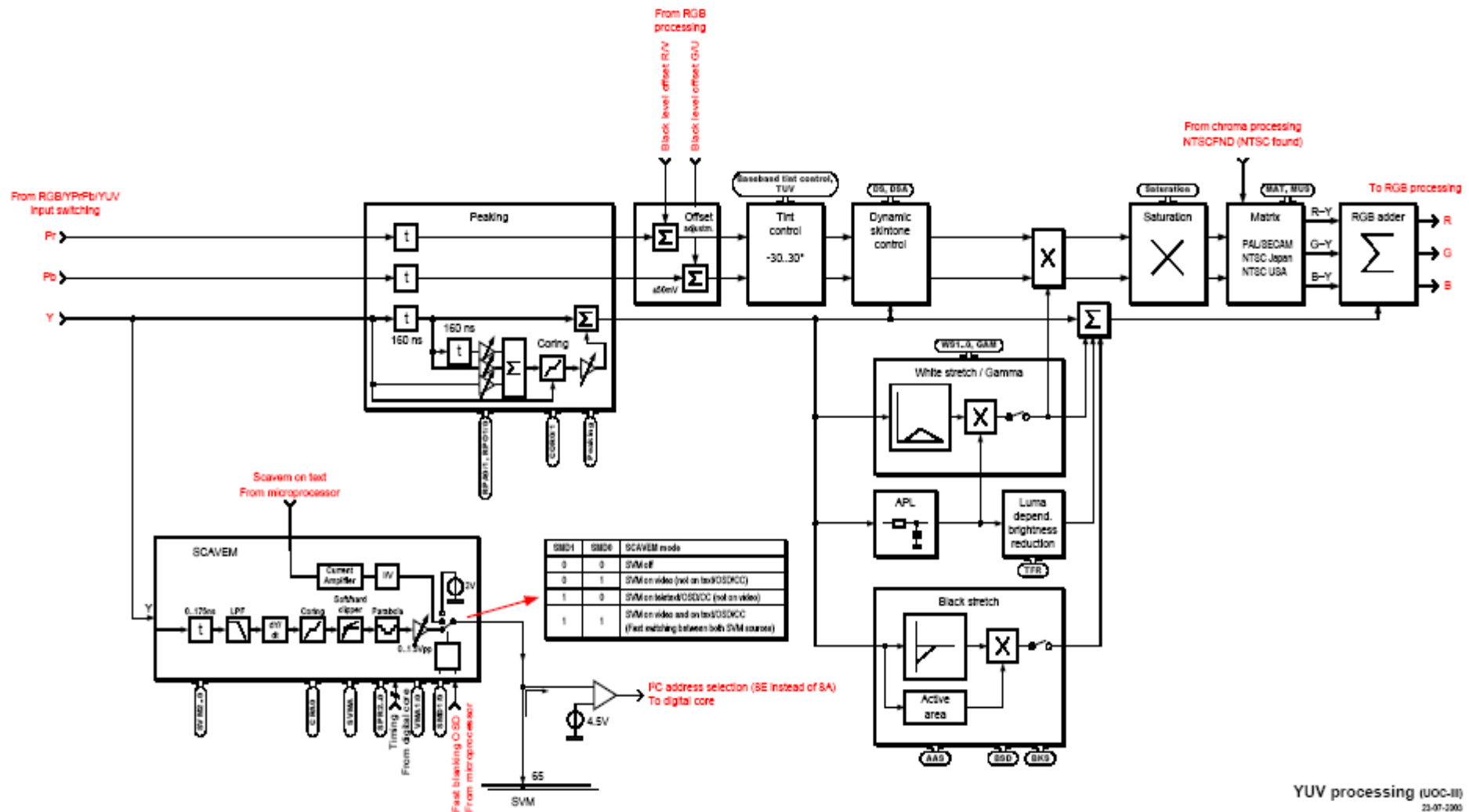
Chroma processing (UOC-III)

20-12-2002

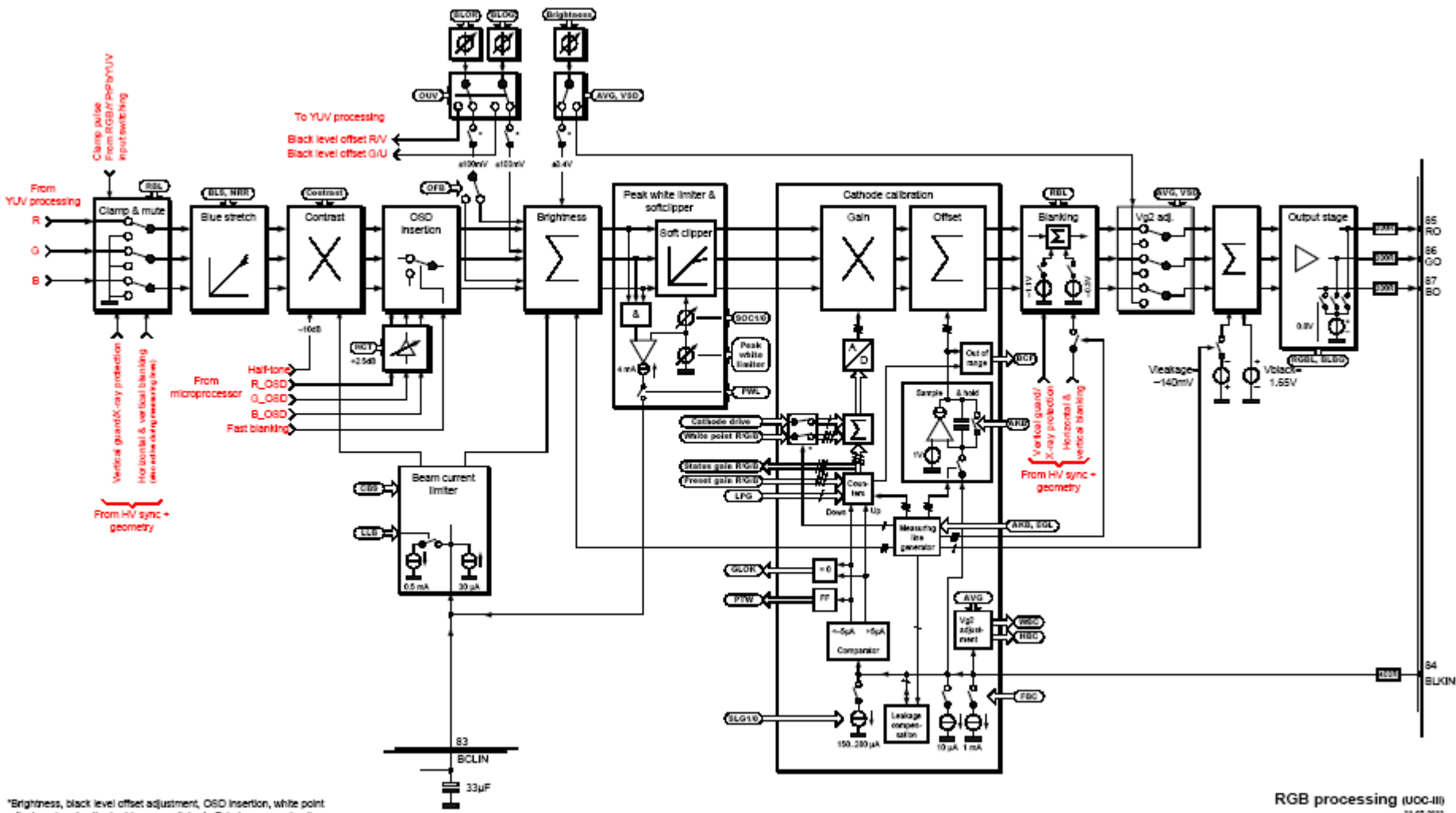
Chroma processing block diagram



YUV processing block diagram



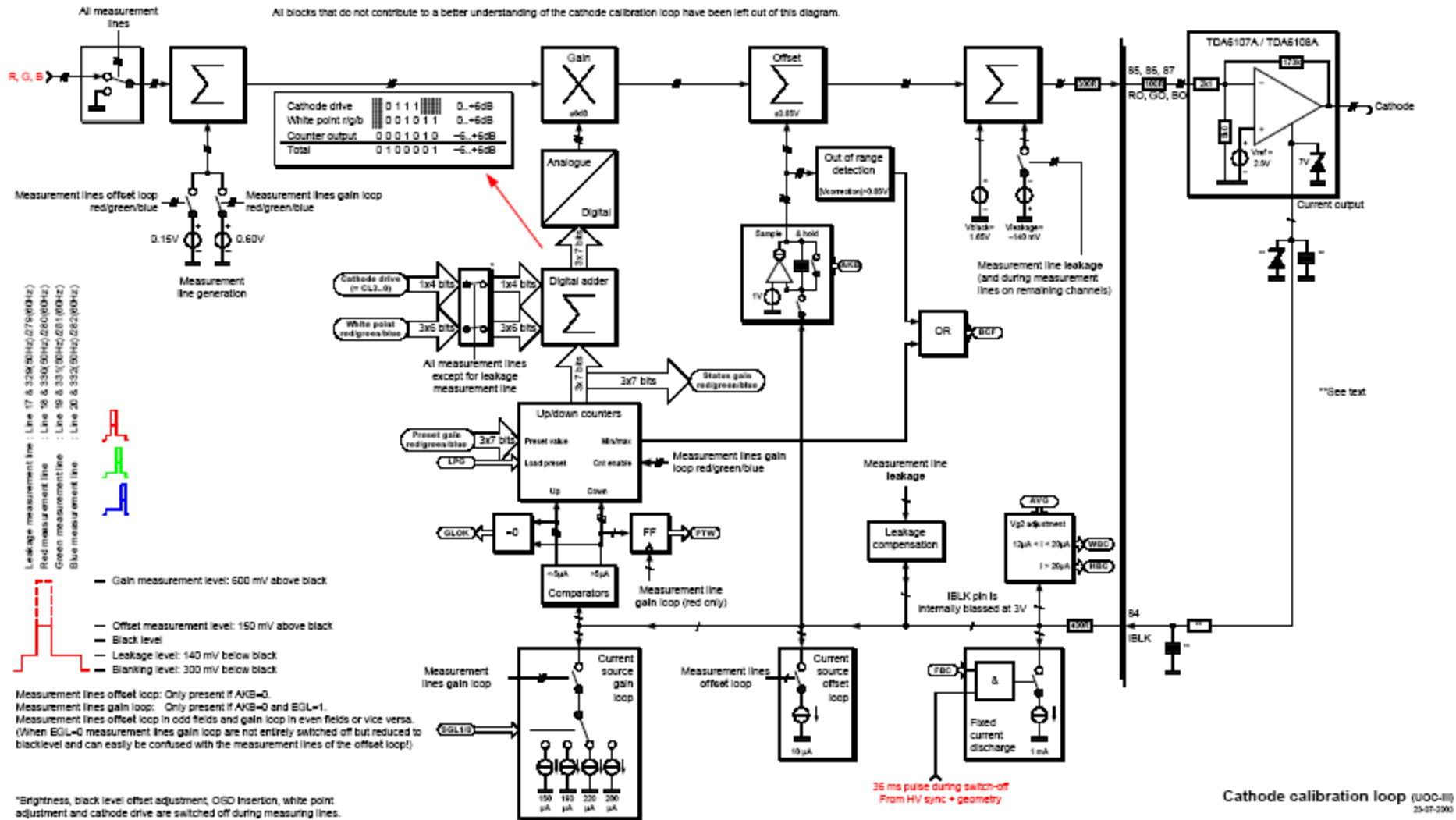
YUV processing (UOC-III)
23-07-2000



*Brightness, black level offset adjustment, OSD insertion, white point adjustment and cathode drive are switched off during measuring lines.

RGB processing (UOC-III)
23-07-2020

Cathode calibration loop block diagram



UOCIII Pinning information

Pin No	Pin configuration(Symbol)	Pinning information(Symbol)	Pin Description(QIP Standard version)
1	VSSC	VSSC/P	Digital ground for m-Controller core and periphery
2	P0.5/INT0//P1.2/INT2	INT0/P0.5	External interrupt 0 or port 0.5(4mA current sinking capability for direct drive of LEDs)
3	VDDC(1.8)/RESET	VDDC4	Digital supply to SDACs(1.8V)
4	P1.0/INT1	P1.0/INT1	Port 1.0 or external interrupt 1
5	P1.1/T0	P1.1/T0	Port 1.1 or Counter/Timer 0 input
6	P1.3/T1	P1.3/T1	Port 1.3 or Counter/Timer 1 input
7	P1.6/SCL	P1.6/SCL	Port 1.6 or I2C-bus clock line
8	P1.7/SDA	P1.7/SDA	Port 1.7 or I2C-bus data line
9	VDDP(3.3V)	VDDP(3.3V)	Supply to periphery and on-chip voltage regulator(3.3V)
10	P2.0/TPMW//P0.4	P2.0/TPWM	Port 2.0 or Tuning PWM output
11	P2.1/PWM0//P0.1	P2.1/PWM0	Port 2.1 or PWM0 output
12	P3.0/ADC0	P3.0/ADC0	Port 3.0 or ADC0 input
13	P3.1/ADC1	P3.1/ADC1	Port 3.1 or ADC1 input
14	P3.2/ADC2	P3.2/ADC2	Port 3.2 or ADC2 input
15	P3.3/ADC3	P3.3/ADC3	Port 3.3 or ADC3 input
16	VDDA3(3.3V)	VDDA3(3.3V),VREF_POS_LSL	Supply(3.3V), positive reference voltage SDAC(3.3V)
17	GND A3	VREF_NEG_LSL+HPL	Negative reference voltage SDAC(0V)
18	XTALIN	XTALIN	Crystal oscillator input
19	XTALOUT	XTALOUT	Crystal oscillator output
20	VSSA1	VSSA1	Ground

UOCIII-N1D series Pinning information

Pin No	Pin configuration(Symbol)	Pinning information(Symbol)	Pin Description(QIP Standard version)
21	DECDIG	DECDIG	Decoupling digital supply
22	VP1	VP1	1st supply voltage TV-processor(+5V)
23	PH2LF	PH2LF	Phase-2 filter
24	PH1LF	PH1LF	Phase-1 filter
25	GND1	GND1	Ground 1 for TV-processor
26	SECPLL	SECPLL	SECAM PLL decoupling
27	DECBG	DECBG	Band gap decoupling
28	VIFIN1	VIFIN1	IF input 1
29	VIFIN2	VIFIN2	IF input 2
30	VSC	VSC	Vertical saw-tooth capacitor
31	IREF	IREF	Reference current input
32	GNDIF	GNDIF	Ground connection for IF amplifier
33	DVBIN1/SIFIN1	SIFIN1/DVBIN1 [2]	SIF input 1/DVB input 1
34	DVBIN2/SIFIN2	SIFIN2/DVBIN2 [2]	SIF input 2/DVB input 2
35	AGCOUT	AGCOUT	Tuner AGC output
36	AMOUT/QSSO/AUDEEM	QSSO/AMOUT/ AUDEEM [2]	QSS inter-carrier output /AM output/De-emphasis (front-end audio out)
37	AUDOUTSL	AUDOUTSL	Audio output for SCART/CINCH(left signal)
38	AUDOUTSR	AUDOUTSR	Audio output for SCART/CINCH(right signal)
39	GND2	GND2	Ground 2 for TV processor
40	PLLIF	PLLIF	IF-PLL loop filter

UOCIII-N1D series Pinning information

Pin No	Pin configuration(Symbol)	Pinning information(Symbol)	Pin Description(QIP Standard version)
41	SIFAGC//DVBAGC	SIFAGC/DVBAGC [2]	AGC sound IF/internal-external AGC for DVB applications
42	DVBO//IFVO/FMRO	DVBO/IFVO/FMRO [2]	Digital Video Broadcast output/IF video output / FM radio output
43	VCC8V	VCC8V	8 Volt supply for audio switches
44	AGC2SIF/SWO/AVL/ SSIF/REFIN/REFO	AVL/SWO/SSIF/REFO/REFIN [2] [3]	Automatic Volume Level-ling/switch output/sound IF input/Sub-carrier reference output/External reference signal input for I signal mixer for DVB operation
45	VP2	VP2	2nd supply voltage TV processor(+5V)
46	SVO/IFVO/CVBSI	IFVO/SVO/CVBSI [2]	IF video output/selected CVBS output/CVBS input
47	AUDIOIN4L//P2.2/PWM1	AUDIOIN4L	Audio-4 input(Left signal)
48	AUDIOIN4R//P2.3/PWM2	AUDIOIN4R	Audio-4 input(Right signal)
49	CVBS4	CVBS4/Y4	CVBS4/Y4 input
50	AUDIOIN2L//P0.2	AUDIOIN2L/SSIF [3]	Audio 2 input(Left signal)/Sound IF input
51	AUDIOIN2R//P0.0	AUDIOIN2R	Audio 2 input(Right signal)
52	CVBS2/Y2	CVBS2/Y2	CVBS2/Y2 input
53	AUDIOIN3L//P1.4/RX/P2.4/PWM3	AUDIOIN3L	Audio 3 input(Left signal)
54	AUDIOIN3R//P1.5/TX/P2.5/PWM4	AUDIOIN3R	Audio 3 input(Right signal)
55	CVBS3/Y3	CVBS3/Y3	CVBS3/Y3 input
56	C2/3	C2/C3	Chroma-2/3 input
57	AUDOUTLSL	AUDOUTLSL	Audio output for audio power amplifier(Left signal)
58	AUDOUTLSR	AUDOUTLSR	Audio output for audio power amplifier(Right signal)
59	AUDOUTHPL	AUDOUTHPL	Audio output for headphone channel(Left signal)
60	AUDOUTHPR	AUDOUTHPR	Audio output for headphone channel(Right signal)

UOCIII-N1D series Pinning information

Pin No	Pin configuration(Symbol)	Pinning information(Symbol)	Pin Description(QIP Standard version)
61	CVBSO/PIP	CVBSO/PIP	CVBS / PIP output
62	VSScomb	VSScomb	Ground connection for comb filter
63	VDDcomb	VDDcomb	Supply voltage for comb filter(+5V)
64	DECSDEM	DECSDEM	Decoupling sound demodulator
65	YSYNC	YSYNC	Y-input for sync separator
66	YOUT	YOUT	Y-output(For YUV interface)
67	INSSW3	INSSW3	3rd RGB/YPBPR insertion input
68	R/PRIN3	R/PRIN3	3rd R input/PR input
69	G/YIN3	G/YIN3	3rd G input/Y input
70	B/PBIN3	B/PBIN3	3rd B input/PB input
71	SVM	SVM	Scan velocity modulation output
72	FBISO/CSY	FBISO/CSY	Flyback input/sandcastle output or composite H/V timing output
73	HOUT	HOUT	Horizontal output
74	EHTO	EHTO	EHT/Overvoltage protection input
75	AVL/EWD	EWD/AVL [1]	East-West drive output or AVL capacitor
76	VDRA	VDRA	Vertical drive A output
77	VDRB	VDRB	Vertical drive B output
78	VGUARD/SWIO		
79	GND3	GND3	Ground 3 for TV-processor
80	VP3	VP3	3rd supply for TV processor

UOCIII-N1D series Pinning information

Pin No	Pin configuration(Symbol)	Pinning information(Symbol)	Pin Description(QIP Standard version)
81	BCLIN	BCLIN	Beam current limiter input
82	BLKIN	BLKIN	Black current input
83	RO	RO	Red output
84	GO	GO	Green output
85	BO	BO	Blue output
86	VDDA1(3.3V)	VDDA1	Analog supply for TCG m-Controller and digital supply for TV-processor(+3.3V)
87	GND A1	VREFAD_NEG	Negative reference voltage(0V)
88	VDDA2(3.3V)	VREFAD_POS	Positive reference voltage(3.3V)
89	VREFAD	VREFAD	Reference voltage for audio ADCs(3.3/2V)
90	VDDA(1.8V)	VDDA(1.8V)	Analogue supply for audio ADCs(1.8V)

- [1] The function of this pin can be chosen by means of the AVLE bit.
- [2] The functional content of these pins is dependent on the mode of operation and on some I2C-bus control bits. More details are given in **"Pin functions for various modes of operation"**.
- [3] The function of pin 33 (face down: 96 and QIP: 44) is controlled by the CMB2-CMB0 bits in subaddress 4AH. When one of the SIF or SSIF functions are selected this selection is overruled by the SSIFS or SSIFM bits (subaddress 35H) when these bits are set to "1". In that case pin 53 (face down: 76 and QIP: 50) is activated as second sound IF input.

Pin functions for various modes of operation

IC MODE	ANALOGUE TV MODE								FM RADIO MODE	
	FM-PLL MODE(QSS =0)		QSS MODE (QSS = 1)							
	FUNCTION		FM DEMODULATION		QSS/AM DEMODULATION		QSS-FM DEMODULATION			
IFA/IFB/IFC bits	000/001/010/011/101/110								101/111	
FMR bit	0		0						1	
FMI bit	-		0						-	
AVLE bit	1	0	1		0		1	0	1	0
CMB2/CMB1/CMB0 bits	000/001/010/011/101/110									
AM bit	-		0	1	0	1	-		-	
Standard QIP										
Pin75	AVL	EWD	AVL		EWD		AVL	EWD	AVL	EWD
Pin33	-		SIFIN1						SIFIN1	
Pin34	-		SIFIN2						SIFIN2	
Pin44 [1]	SWO/ SSIF/ REFO	AVL/ SWO/ SSIF/ REFO	SWO/ SSIF/ REFO		AVL/ SWO/ SSIF/ REFO		SWO/ SSIF/ REFO	AVL/ SWO/ SSIF/ REFO	SWO/ SSIF/ REFO	AVL/ SWO/ SSIF/ REFO
pin36/-	AUDEEM		QSSO	AMOUT	QSSO	AMOUT	AUDEEM		AUDEEM	
pin41	-		SIFAGC						SIFAGC	
Pin42[2]	IFVO		IFVO						FMRO	
pin46[3]	IFVO/SVO/CVBSI		IFVO/SVO/CVBSI						IFVO/SVO/CVBSI	
pin59[4]	AUDOUT		AUDOUT	AMOUT	AUDOUT	AMOUT	AUDOUT		AUDOUT	

[1] The function of this pin is controlled by the bits CMB2-CMB0 in subaddress 4AH.

[2] The functions of the pins 43/44 (standard pinning) or 85/86 (face-down pinning) are controlled by the IFO2-IFO0 bits in subaddress 31H.

[3] The function of this pin is determined by the SVO1/SVO0 bits in subaddress 39H.

[4] This functionality is only valid for the mono versions. In the "stereo" and "AV-stereo" versions this pin has the function of audio output for the headphone channel (left signal).

Analogue Video Processing (all versions)

- ◆ Multi-standard vision IF circuit with alignment-free PLL demodulator
- ◆ Internal (switchable) time-constant for the IF-AGC circuit
- ◆ Switchable group delay correction and sound trap (with switchable centre frequency) for the demodulated CVBS signal
- ◆ DVB/VSB IF circuit for preprocessing of digital TV signals.
- ◆ Video switch with 3 external CVBS inputs and a CVBS output. All CVBS inputs can be used as Y-input for Y/C signals. However, only 2 Y/C sources can be selected because the circuit has 2 chroma inputs. It is possible to add an additional CVBS(Y)/C input(CVBS/YX and CX) when the YUV interface and the RGB/YPBPR input are not needed. The QIP90 versions have only 2 CVBS inputs, one chroma input and no YUV interface.
- ◆ Automatic Y/C signal detector
- ◆ Adaptive digital (4H/2H) PAL/NTSC comb filter for optimum separation of the luminance and the chrominance signal.
- ◆ Integrated luminance delay line with adjustable delay time
- ◆ Picture improvement features with peaking (with switchable centre frequency, depeaking, variable positive/negative peak ratio, variable pre-/overshoot ratio and video dependent coring), dynamic skin tone control, gamma control and blue- and black stretching. All features are available for CVBS, Y/C and RGB/YPBPR signals.
- ◆ Switchable DC transfer ratio for the luminance signal
- ◆ Only one reference (24.576 MHz) crystal required for the TCG m-Controller, digital sound processor, Teletext- and the colour decoder
- ◆ Multi-standard colour decoder with automatic search system and various "forced mode" possibilities
- ◆ Internal base-band delay line
- ◆ Indication of the Signal-to-Noise ratio of the incoming CVBS signal
- ◆ Linear RGB/YPBPR input with fast insertion.
- ◆ YUV interface. When this feature is not required some pins can be used as additional RGB/YPBPR input. It is also possible to use these pins for additional CVBS (or Y/C) input (CVBS/YX and CX). The QIP90 version has no YUV interface.
- ◆ Tint control for external RGB/YPBPR signals
- ◆ Scan Velocity Modulation output. The SVM circuit is active for all the incoming CVBS, Y/C and RGB/YPBPR signals. The SVM function can also be used during the display of teletext pages.
- ◆ RGB control circuit with 'Continuous Cathode Calibration', white point and black level off-set adjustment so that the colour temperature of the dark and the light parts of the screen can be chosen independently.
- ◆ Contrast reduction possibility during mixed-mode of OSD and Text signals
- ◆ Adjustable 'wide blanking' of the RGB outputs
- ◆ Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- ◆ Vertical count-down circuit
- ◆ Vertical driver optimized for DC-coupled vertical output stages
- ◆ Horizontal and vertical geometry processing with horizontal parallelogram and bow correction and horizontal and vertical zoom
- ◆ Low-power start-up of the horizontal drive circuit

Analogue video processing

1 Stereo versions

- ◆ The low-pass filtered 'mixed down' I signal is available via a single ended or balanced output stage. The QIP90 versions have only a single ended output.

2 Mono versions

- ◆ The low-pass filtered 'mixed down' I signal is available via a single ended output stage

3 Digital Video Processing (some versions)

- ◆ Double Window mode applications. It is possible to display a video and a text window or 2 text windows in parallel.
- ◆ Linear and non-linear horizontal scaling of the video signal to be displayed.

Description of the I2C-bus subaddresses

Function	Subaddr (hex)	Data byte								POR Value
		D7	D6	D5	D4	D3	D2	D1	D0	
Spare	00	0	0	0	0	0	0	0	0	00
Spare	01	0	0	0	0	0	0	0	0	00
Spare	02	0	0	0	0	0	0	0	0	00
Volume control (L)	03	0	A6	A5	A4	A3	A2	A1	A0	20
Volume control R [2]	04	0	A6	A5	A4	A3	A2	A1	A0	20
Horizontal shift (HS)	05	0	0	A5	A4	A3	A2	A1	A0	20
Horizontal parallelogram[PAR]	06	0	0	A5	A4	A3	A2	A1	A0	20
Horizontal bow[BOW]	07	0	0	A5	A4	A3	A2	A1	A0	20
Vertical linearity[VL]	08	VL1	VL0	A5	A4	A3	A2	A1	A0	20
Vertical scroll	09	0	0	A5	A4	A3	A2	A1	A0	20
EW width (EW) [1]	0A	0	0	A5	A4	A3	A2	A1	A0	20
EW parabola/width (PW) [1]	0B	0	0	A5	A4	A3	A2	A1	A0	20
EW upper corner parabola [1]	0C	0	0	A5	A4	A3	A2	A1	A0	20
EW lower corner parabola [1]	0D	0	0	A5	A4	A3	A2	A1	A0	20
EW trapezium (TC) [1]	0E	0	0	A5	A4	A3	A2	A1	A0	20
Vertical slope (VS)	0F	0	0	A5	A4	A3	A2	A1	A0	20
Vertical amplitude (VA)	10	0	0	A5	A4	A3	A2	A1	A0	20
S-correction (SC)	11	0	0	A5	A4	A3	A2	A1	A0	20
Vertical shift (VSH)	12	0	0	A5	A4	A3	A2	A1	A0	20
Vertical zoom (VX)	13	0	0	A5	A4	A3	A2	A1	A0	20
Off-set IF demodulator	14	0	0	A5	A4	A3	A2	A1	A0	20
AGC take-over	15	0	0	A5	A4	A3	A2	A1	A0	20

Description of the I2C-bus subaddresses

Function	Subaddr (hex)	Data byte								POR Value
		D7	D6	D5	D4	D3	D2	D1	D0	
Spare	16	0	0	0	0	0	0	0	0	00
Black level offset R	17	0	0	A5	A4	A3	A2	A1	A0	20
Black level offset G	18	0	0	A5	A4	A3	A2	A1	A0	20
Peaking	19	PF1	PF0	A5	A4	A3	A2	A1	A0	20
White limiting	1A	0	0	SOC1	SOC0	A3	A2	A1	A0	08
Brightness	1B	0	0	A5	A4	A3	A2	A1	A0	20
Saturation	1C	0	0	A5	A4	A3	A2	A1	A0	20
Contrast	1D	0	0	A5	A4	A3	A2	A1	A0	20
Base-band tint control	1E	0	0	A5	A4	A3	A2	A1	A0	20
Spare	1F	0	0	0	0	0	0	0	0	00
White point R	20	0	0	A5	A4	A3	A2	A1	A0	00
White point G	21	0	0	A5	A4	A3	A2	A1	A0	00
White point B	22	0	0	A5	A4	A3	A2	A1	A0	00
PGR - Preset Gain Red	23	LPG	A6	A5	A4	A3	A2	A1	A0	00
PGG - Preset Gain Green	24	0	A6	A5	A4	A3	A2	A1	A0	00
PGB - Preset Gain Blue	25	0	A6	A5	A4	A3	A2	A1	A0	00
Timing of 'wide blanking' [1]	26	WBF3	WBF2	WBF1	WBF0	WBR3	WBR2	WBR1	WBR0	88
Hue for NTSC	27	0	0	A5	A4	A3	A2	A1	A0	00
IF Preset Value 1	28	0	EPVI	A5	A4	A3	A2	A1	A0	00
IF Preset Value 2	29	0	0	A5	A4	A3	A2	A1	A0	00
Spare	2A	0	0	0	0	0	0	0	0	00
Spare	2B	0	0	0	0	0	0	0	0	00

Description of the I2C-bus subaddresses

Function	Subaddr (hex)	Data byte								POR Value
		D7	D6	D5	D4	D3	D2	D1	D0	
Spare	2C	0	0	0	0	0	0	0	0	00
Spare	2D	0	0	0	0	0	0	0	0	00
Spare	2E	0	0	0	0	0	0	0	0	00
Vision IF 0	2F	AFG	IFD	IFA	IFB	IFC	VSW	MOD	AFN	00
Vision IF 1	30	0	STM	AGCM	IFLF	GD	AGC1	AGC0	FFI	00
Vision IF 2	31	CMSS	VA1	VA0	VAI	IFS	IFO2	IFO1	IFO0	00
Sound 0	32	TYUV1	NRR	BPBS	DSG	RDS	MONO	FMWS1	FMWS0	00
Sound 1	33	AGN	AM	SM1	SM0	FMD	FMC	FMB	FMA	00
Sound 2	34	0	0	AVLE	QSS	BPB	AVL[4]	FMR	FMI	00
Sound 3	35	0	FMS	AVLM	SSIFS	SSIFM	CMCA	BPB2	AMLOW	00
Audio selection 0	36	CLF	HPVC	SPT	0	SMLS	SO2	SO1	SO0	00
Audio selection 1	37	0	E2D[3]	SAS2	SAS1	SAS0	HPO2	HPO1	HPO0	00
Video selection 0	38	CS1A	CS1B	CS1C	CS1D	INA	INB	INC	IND	00
Video selection 1	39	BWYC[5]	CFA2[5]	CFA1[5]	CFA0[5]	CV2	SVO1	SVO0	SYS	00
Video selection 2	3A	CBPS	0	VDXEN	VDX	YD3	YD2	YD1	YD0	00
Colour decoder 0	3B	CM3	CM2	CM1	CM0	MAT	MUS	ACL	CB	00
Colour decoder 1	3C	SBO1	SBO0	CHSE1	CHSE0	CLO	DTR	BPS	FCO	00
Synchronisation 0	3D	SDC	HP2	FOA	FOB	POC	STB	HTXT	VID	00
Synchronisation 1	3E	WBI	RED	FSL	OSO	FORF	FORS	DL	NCIN	00
Synchronisation 2	3F	SLD	VGM1	VGM0	LED	SSL	SD2	SD1	SD0	00
Deflection 0	40	VSD	OSVE	DFL	XDT	SBL	AVG	EVG	HCO[1]	00
Deflection 1 / Control 0	41	DEFL	SVMA	MVK	OSB	BKC	TYUV0	FBC	EVB	00

Description of the I2C-bus subaddresses

Function	Subaddr (hex)	Data byte								POR Value
		D7	D6	D5	D4	D3	D2	D1	D0	
Control 1	42	INTF	EGL	SLG0	AKB	CL3	CL2	CL1	CL0	00
Control 2	43	IE3	IE2	DINT	YC	YUV2	YUV1	YUV0	HBL ^[1]	00
Control 3	44	GAM	TFR	CLD	CBS	OUV	PWL	RBL	RGBL	00
Control 4	45	BKS	BSD	AAS0	DSK	WS1	WS0	BLS	TUV	00
Control 5	46	OFB	HCT	FINM	FIN	SLG1	BLBG	LLB	DSA	00
Peaking	47	BPD	0	RPA1	RPA0	RPO1	RPO0	COR1	COR0	00
SVM 0	48	COFF	CRA0	SPR2	SPR1	SPR0	SVM2	SVM1	SVM0	00
SVM 1	49	DSS	0	TXTLV1	TXTLV0	VMA1	VMA0	SMD1	SMD0	00
Miscellaneous 1	4A	QDT	DISG	DDLE	LCD	SWO1	CMB2	CMB1	CMB0	00
Miscellaneous 2	4B	AAS1	FBC1	PDCM	0	BPYD ^[5]	0	0	0	00
Miscellaneous 3	4C	0	0	0	0	TCI2X	TCCON	0	TXTS	00

^[1] These functions are only available when the East-West drive output is active (AVLE = 0).

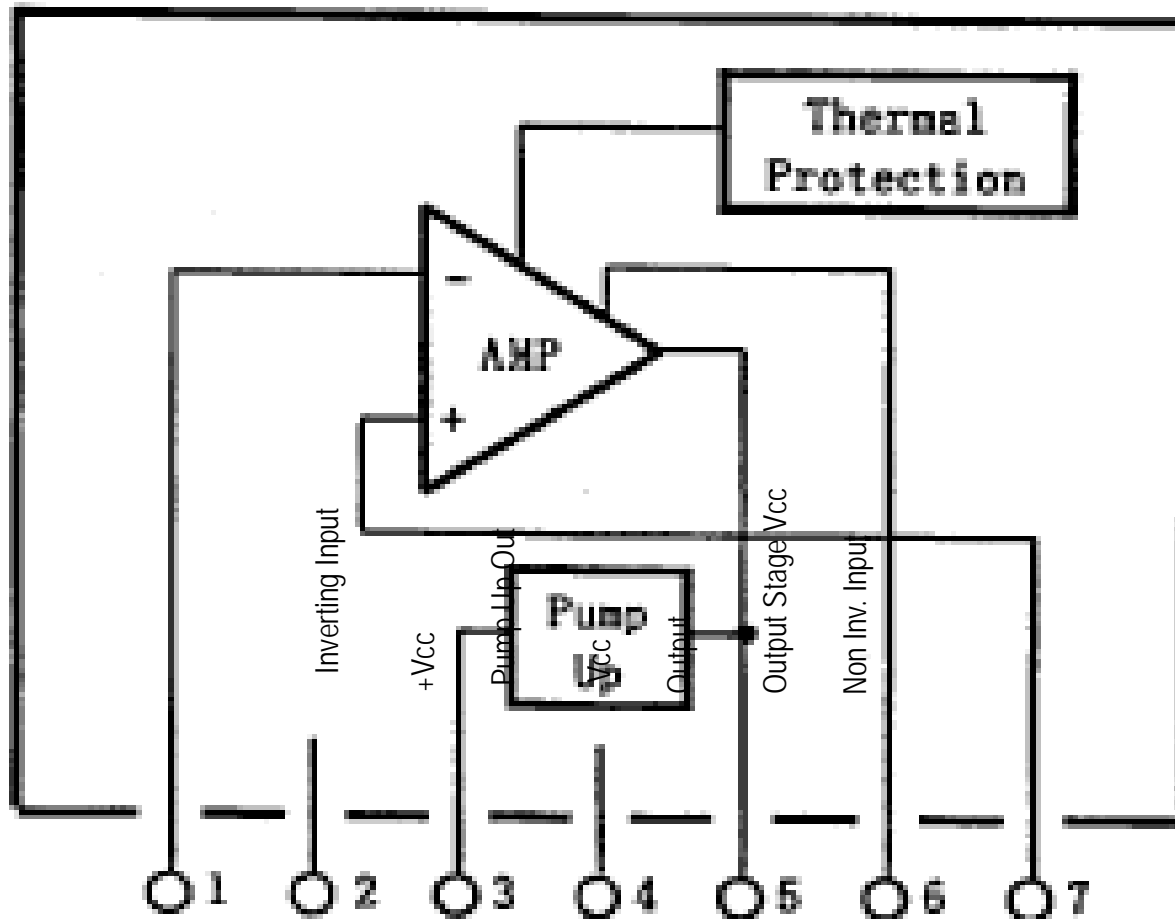
^[2] This function is available only in the "Stereo" and "AV Stereo" versions.

^[3] Only available in the "Mono" versions

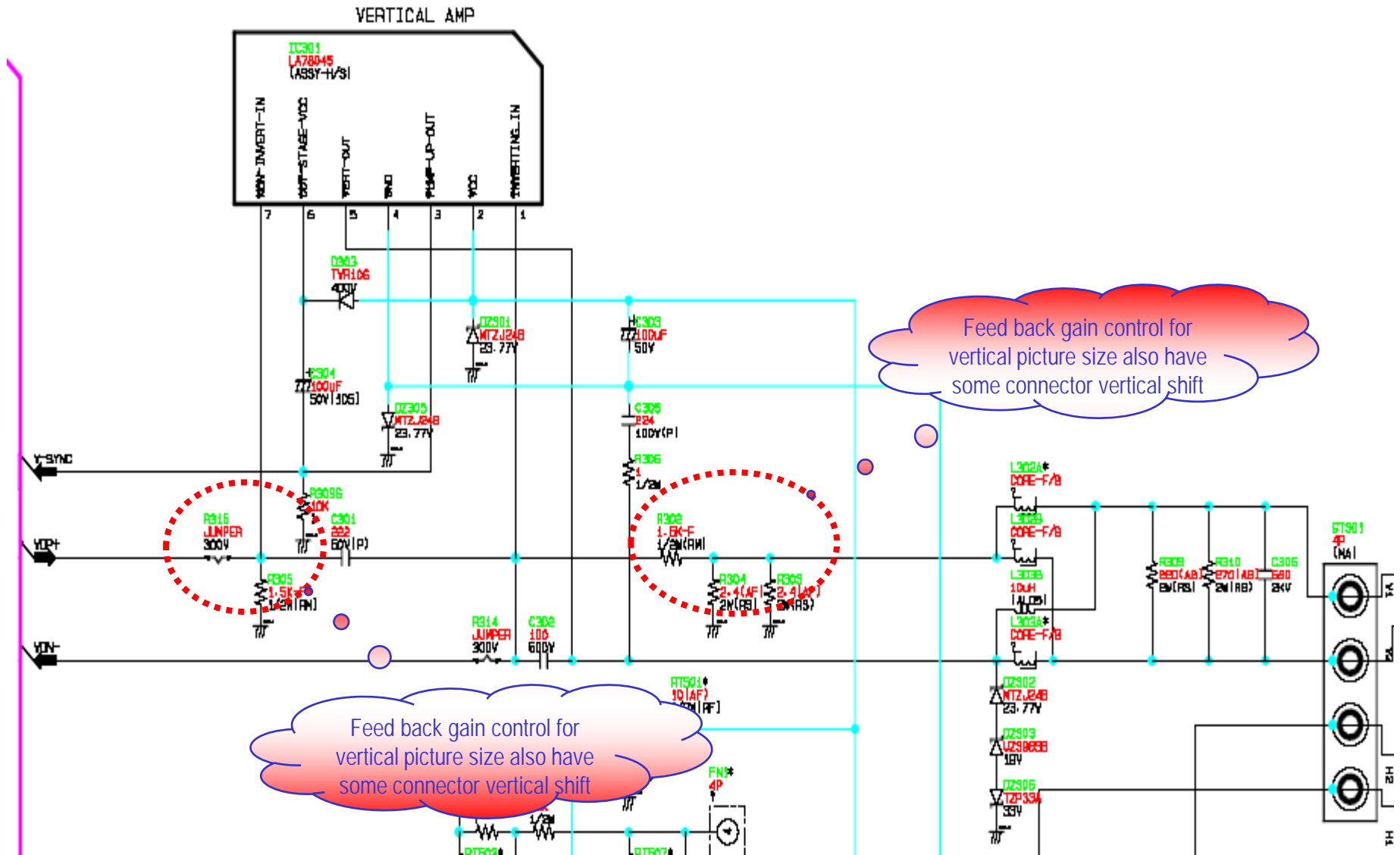
^[4] The AVL function can only be activated when a capacitor is connected to the EW output pin (AVLE = 1) or to the subcarrier output pin(via the bits CMB2-CMB0).

^[5] These bits are valid only for versions with 2-D comb filter

LA78045 Vertical IC Block Diagram

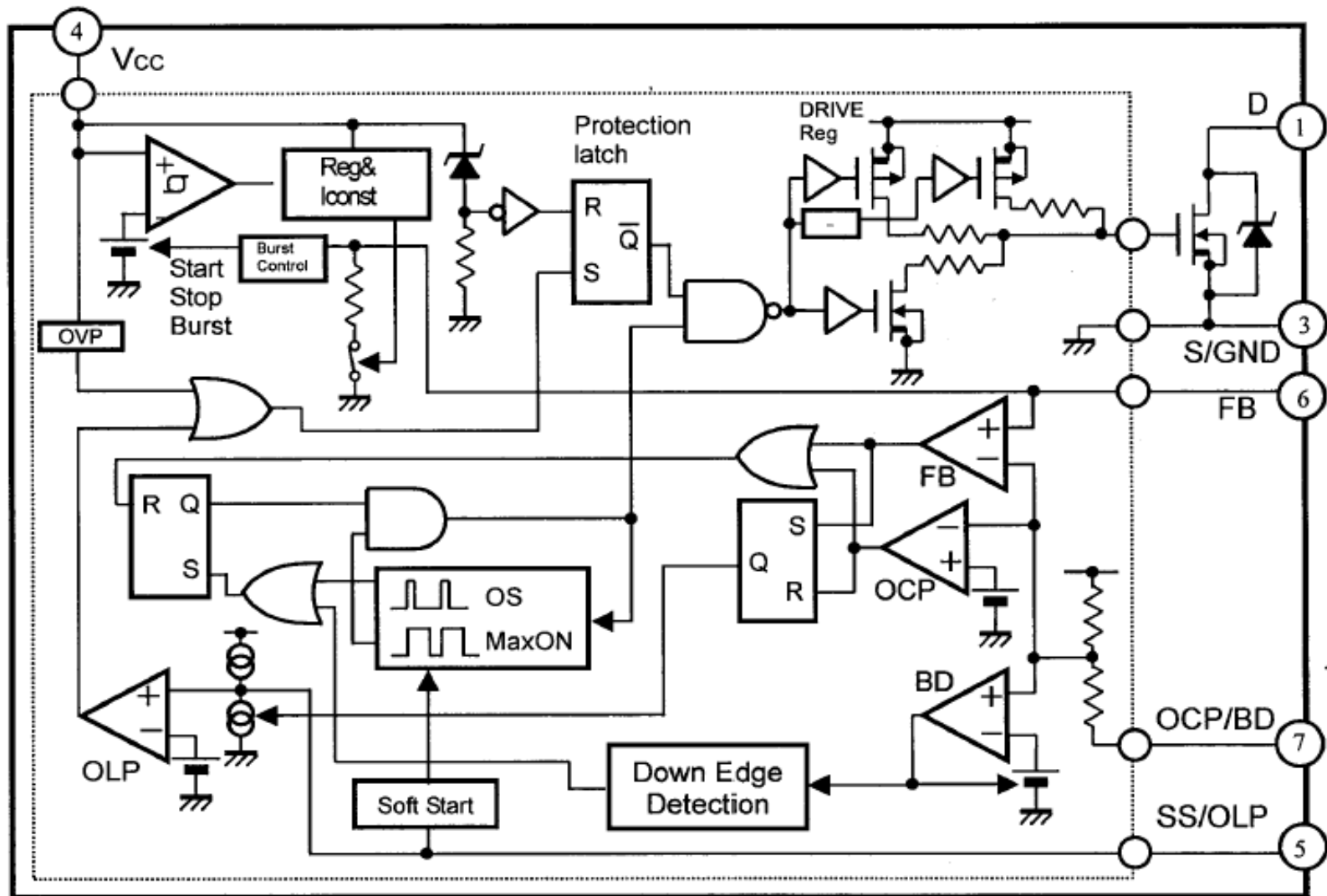


Vertical

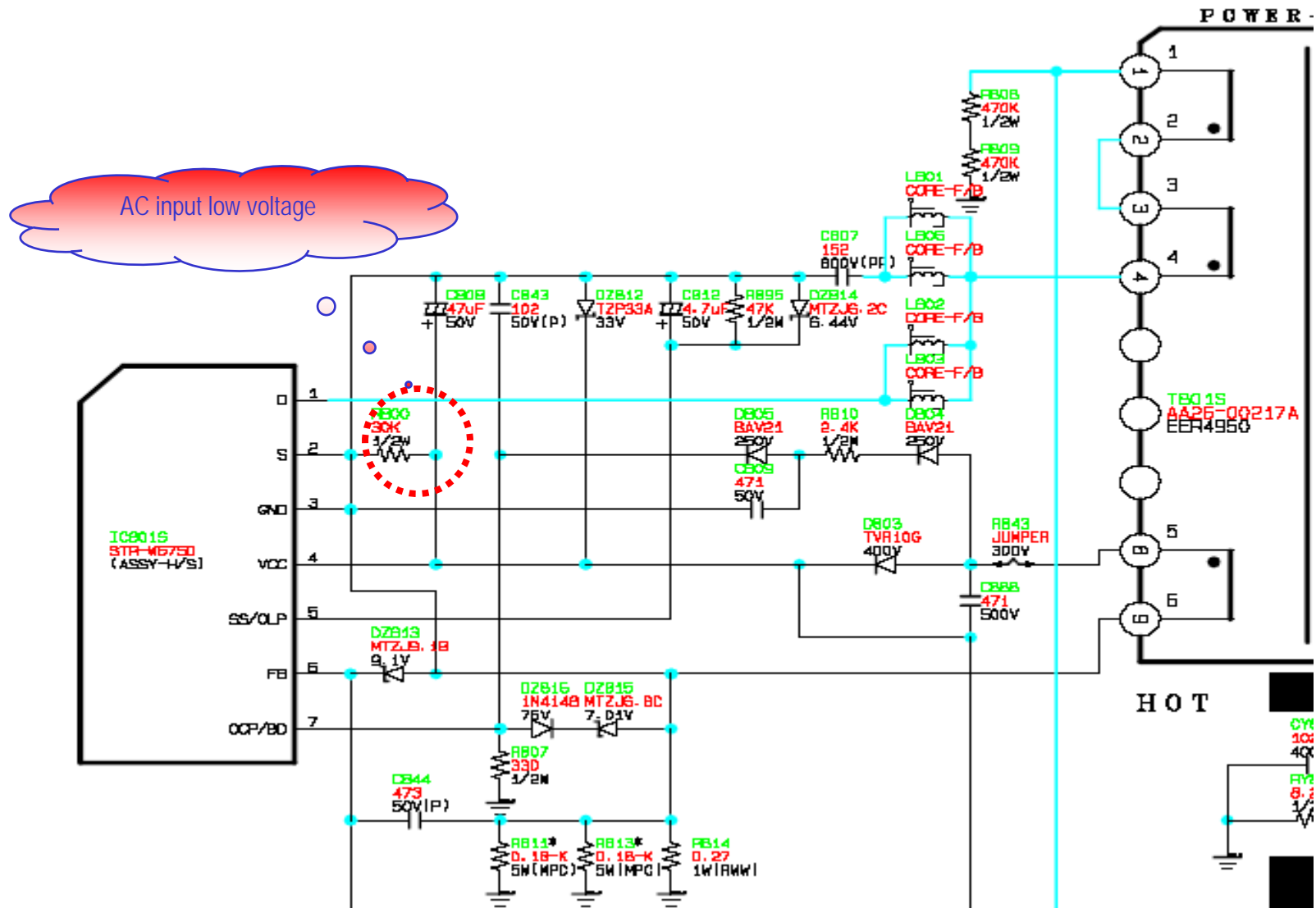


STR-W6750F Power IC Block Diagram

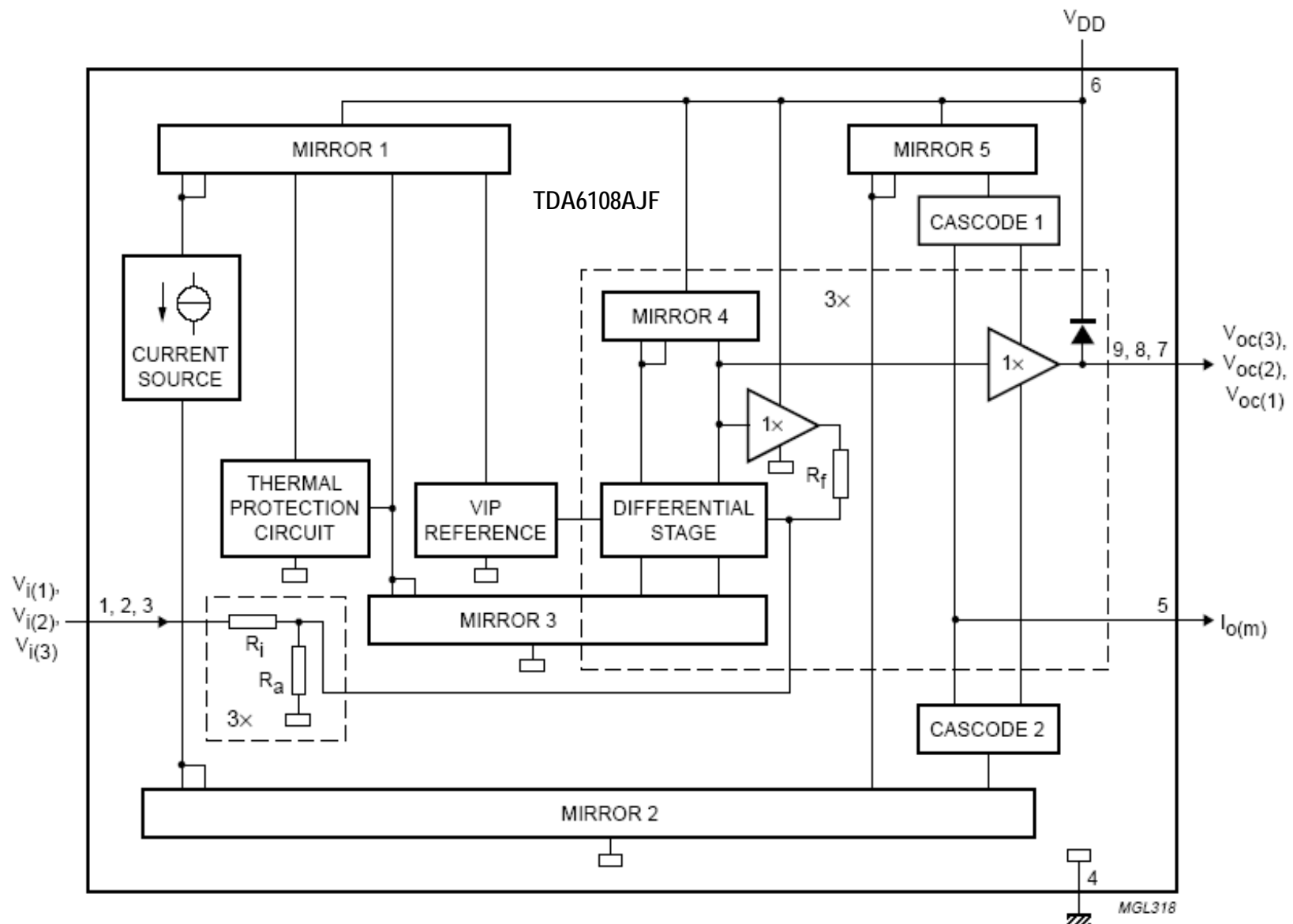
Block diagram (Connection diagram)



STR-W6750F Power



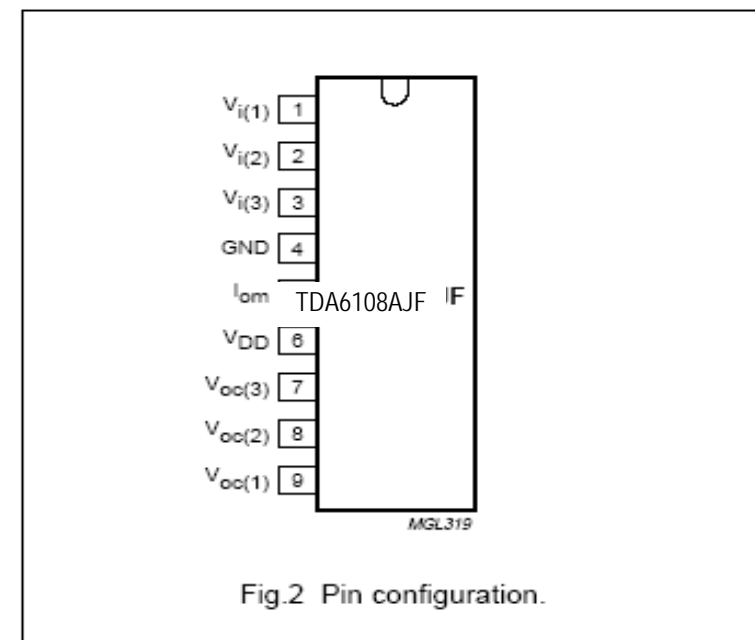
TDA6108AJF Block diagram (one amplifier shown)



TDA6108AJF Block diagram (one amplifier shown).

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i(1)}$	1	inverting input 1
$V_{i(2)}$	2	inverting input 2
$V_{i(3)}$	3	inverting input 3
GND	4	ground (fin)
I_{om}	5	black current measurement output
V_{DD}	6	supply voltage
$V_{oc(3)}$	7	cathode output 3
$V_{oc(2)}$	8	cathode output 2
$V_{oc(1)}$	9	cathode output 1



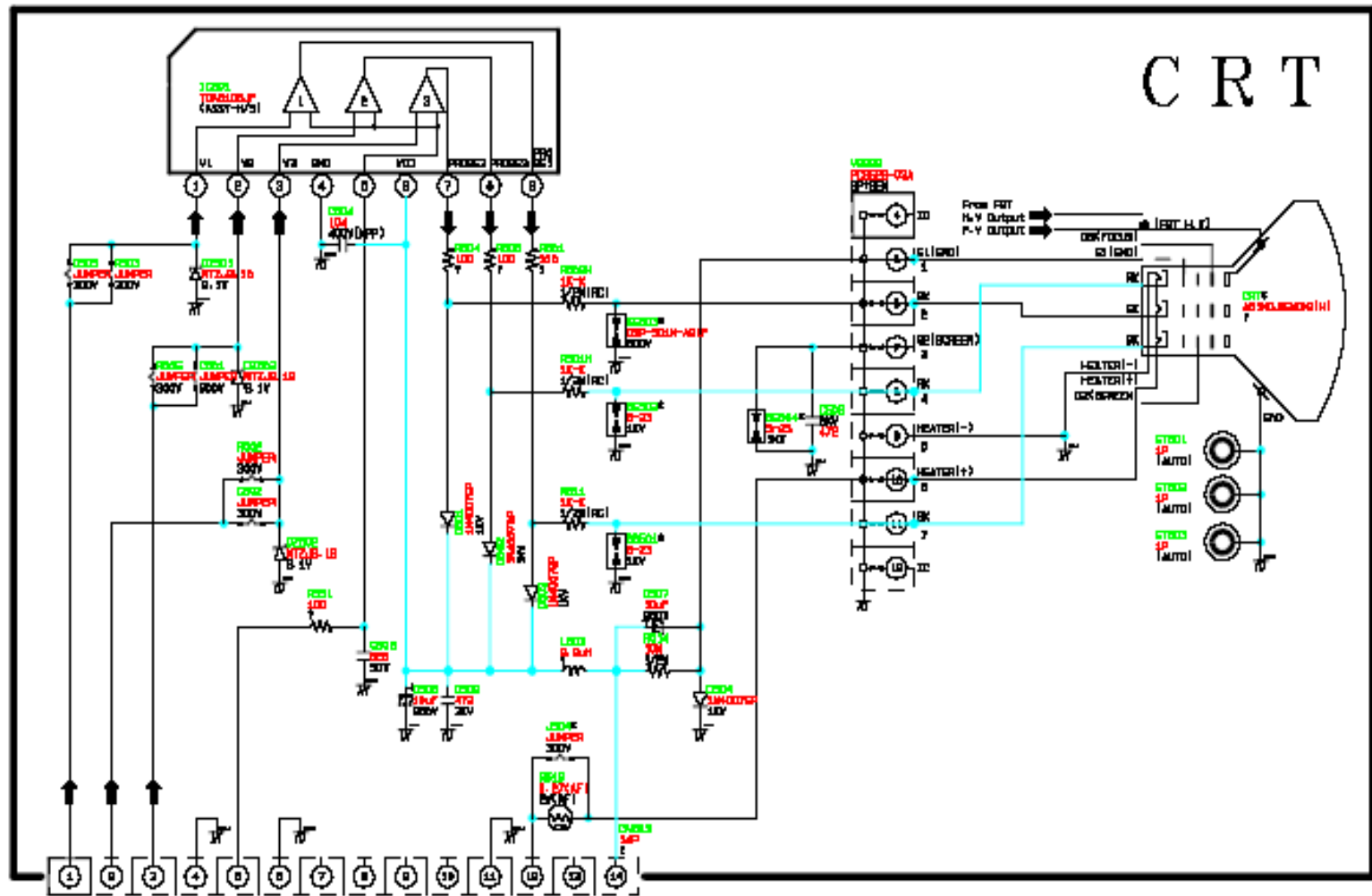
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages measured with respect to pin 4 (ground); currents as specified in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		0	250	V
V_i	input voltage		0	12	V
V_{om}	measurement output voltage		0	6	V
V_{oc}	cathode output voltage		0	V_{DD}	V
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-20	+150	°C
V_{es}	electrostatic handling				
	human body model (HBM)		-	2000	V
	machine model (MM)		-	300	V

CRT Drive

✂ In order to Drive the CRT, the signal of Red, Green, Blue are amplified.



UOCIII & VCT-IF Difference Function

BLOCK	MAKERS	PHILIPS UOC2	TOSHIBA 2IN1	MICRONAS VCT-IF		PHILIPS UOC3
	FEATURES	TDA9351	TMPA8801	ECONOMIC	BASIC	Stereo QIP90
VCD	System	Multi	Multi	Multi	Multi	Multi
	CVBS Input(Include RF)	2	2	4	4	4 (3) (2)
	SVHS(C IN)	1	1	2	2	0 (1) (2)
	Contrast control	Y	Y	Y	Y	Y
	Bright control	Y	Y	Y	Y	Y
	Tint control	Y	Y	Y	Y	Y
	Sharpness control	Y	Y	Y	Y	Y
	Saturation control	Y	Y	Y	Y	Y
	Blue stretch	N	N	Y	Y	Y
	Black stretch	Y	Y	Y	Y	Y
	White stretch	N	N	N	N	Y
	EW (EHT HV)	Y	Y	Y	Y	Y
	Coring	N	Y	Y	Y	Y
	Scart (CVBS OUT)	1	1	1	3	2
	Comb Filter	1H	1H	1H	4H	2H/4H
	DVD(Y Pb Pr 1H)	N	1	1	1	1
	AKB(Cutoff) High light ?(Switchable AKB On/Off)	Y	Y(S/W)	Y	Y	Y
	Vertical Zoom Deflection	Y	Y	Y	Y	Y
	CTI	N	N	N	Y	N
	LTI	N	N	N	Y	N
	SVM (Scan Velocity Modulation)	N	Y	N	Y	Y

UOCIII & VCT-IF Difference Function

BLOCK	MAKERS	PHILIPS UOC2	TOSHIBA 2IN1	MICRONAS VCT-IF		PHILIPS UOC3
	FEATURES	TDA9351	TMPA8801	ECONOMIC	BASIC	Stereo QIP90
VCD	Horiz Scaler (Panorama)	N	N	N	Y	Y
	Horiz Scaler (Panorama) RGB	N	N	N	Y	Y
	Double Focus out	N	N	Dynamic Focus	Dynamic Focus	Dynamic Focus
	Auto Wide(Black Line)	N	N	N	Y	N
	Histogram	N	N	N	Y	N
	PC input (VGA, SVGA, XGA)	N	N	N	N	N
	RGB F/B input	Y	Y	Y	Y	Y
	Angle & Bow	N	N	Y	Y	Y
	Soft start stop	Y	??	Y	Y	Y
	SNR measurement(CVBS)	N	N	Y(BIT??)	Y(BIT??)	Y(2-BIT)
	White Balance Control	Y	Y	Y	Y	Y
	ABL (Average Beam Limiter)	Y	Y	Y	Y	Y
	Test Pattern Generator	N	Y	Y	Y	N

UOCIII & VCT-IF Difference Function

BLOCK	MAKERS	PHILIPS UOC2	TOSHIBA 2IN1	MICRONAS VCT-IF		PHILIPS UOC3
	FEATURES	TDA9351	TMPA8801	ECONOMIC	BASIC	Stereo QIP90
SOUND	Input	1	Mono1	MO 2	Stereo 2 (3)	3
	Out put	1	Mono1	MO 1	Stereo 2 (1)	1
	Out put Speaker	1	Mono1	MO 1	Stereo 1	1
	AM	Y	N	Y	Y	Y
	FM 4.5	Y	Y	Y	Y	Y
	FM 5.5, 6.0, 6.5	Y	Y	Y	Y	Y
	Dual mono 4.72, 5.74	N	Y	Y	Y	Y
	FM Radio mono	N	N	Y	Y	Y
	Volume control mono	Y	Y	Y	Y	N
	Bass on/off mono	N	N	Y	Y	Y
	Treble on/off mono	N	N	Y	Y	Y
	Pseudo Stereo	N	N	N	Y	N
	BBE					Y
	Melody on/off	N	N	??	Y	Y
	Switchable AVL mono	Y	N	Y	Y	Y
	RDS	N	N	Y	Y	Y
	Micronas Dynamic Bass	N	N	Y	Y	Dynamic Bass
	Dynamic Bass Enhancement	N	N	N	N	Y
	Line Stereo (AV Stereo)	N	N	N	Y	Y
	Balance	N	N	N	Y	Y
	Virtual Dolby	N	N	N	Y	Y

UOCIII & VCT-IF Difference Function

BLOCK	MAKERS	PHILIPS UOC2	TOSHIBA 2IN1	MICRONAS VCT-IF		PHILIPS UOC3
	FEATURES	TDA9351	TMPA8801	ECONOMIC	BASIC	Stereo QIP90
SOUND	VIP Sound	N	N	N	Y	N
	A2 Stereo	N	N	N	Y	Y
	Nicam Stereo	N	N	N	Y	Y
	MTS(JPN, USA)	N	N	N	Y	Y
	Equalizer	N	N	N	Y	Y
	Dolby Prologic	N	N	N	N	N
	Dolby Digital AC3	N	N	N	N	N
	Head Phone Volume	N	N	N	N	Y

UOCIII & VCT-IF Difference Function

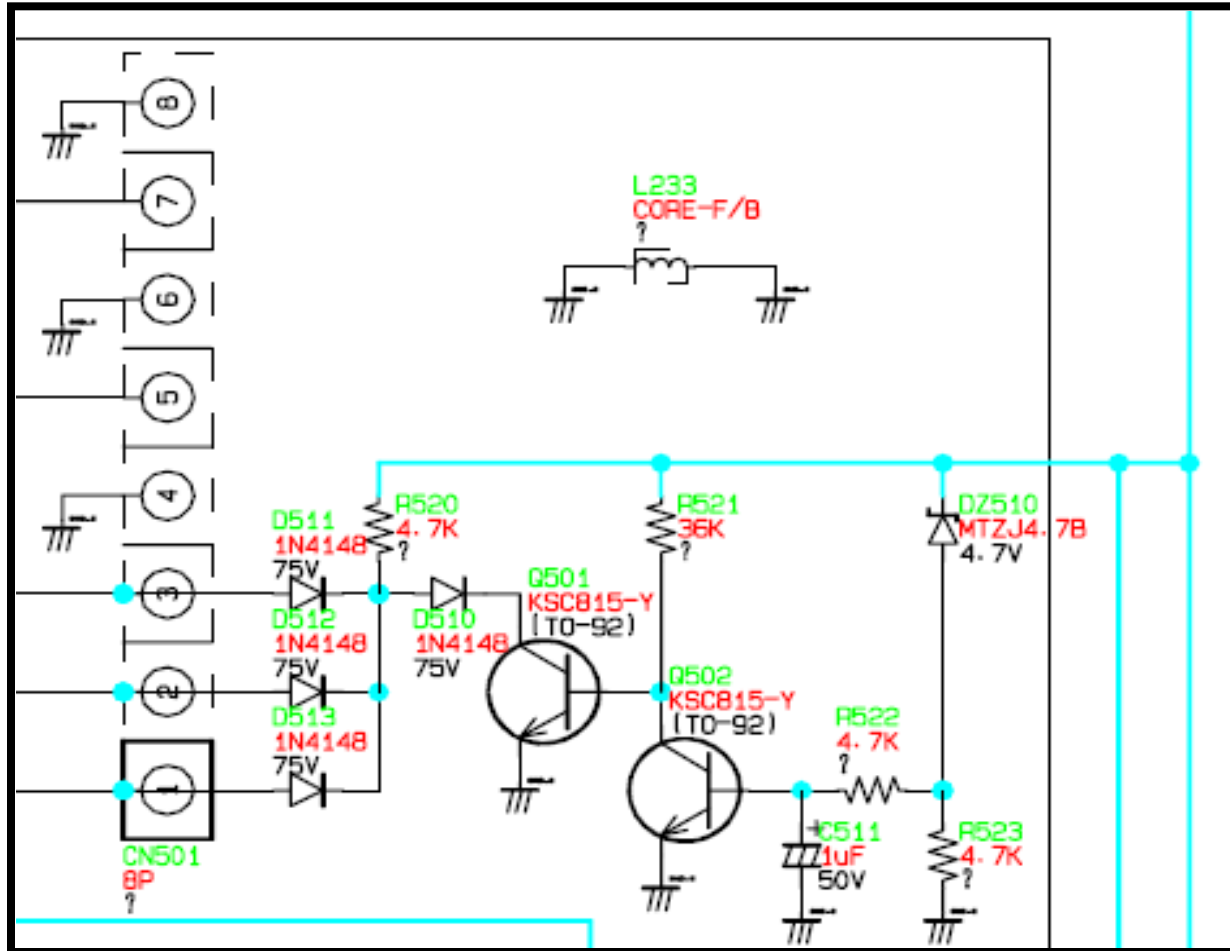
BLOCK	MAKERS	PHILIPS UOC2	TOSHIBA 2IN1	MICRONAS VCT-IF		PHILIPS UOC3
	FEATURES	TDA9351	TMPA8801	ECONOMIC	BASIC	Stereo QIP90
PIP	Double Text(RF+TTX)	N	N	N	Y	N

BLOCK	MAKERS	PHILIPS UOC2	TOSHIBA 2IN1	MICRONAS VCT-IF		PHILIPS UOC3
	FEATURES	TDA9351	TMPA8801	ECONOMIC	BASIC	Stereo QIP90
TTX & CCD	TTX 10 page	Y	N	Y	Y	Y
	TTX 100 page	N	N	N	Y(Ext Memory)	Option
	Hi-Text 2.5	N	N	N	N	N
	caption korean	N	N	N	N	Y
	caption US	Y	Y	Y	Y	Y
	US V-Chip	Y	Y	Y	Y	Y
	Canadian V-Chip	??	Y	Y	Y	??
	Auto Clock Set (ACS)	??	Y	Y	Y	??

BLOCK	MAKERS	PHILIPS UOC2	TOSHIBA 2IN1	MICRONAS VCT-IF		PHILIPS UOC3
	FEATURES	TDA9351	TMPA8801	ECONOMIC	BASIC	Stereo QIP90
MICOM	EPG	N	N	N	N	N
	ROM Size (Byte)	64K	48K	128Kbyte	256Kbyte	128K/256K
	RAM Size (Byte)	1K	2K	8K	8K	4K/8K
	Font Matrix	12X10,12X13, 12X16		16X18 (Optional 12X10)		12X(9,10,13,16) 16X18
	Character Size		16X18	512 Characters (16X18)		16X18

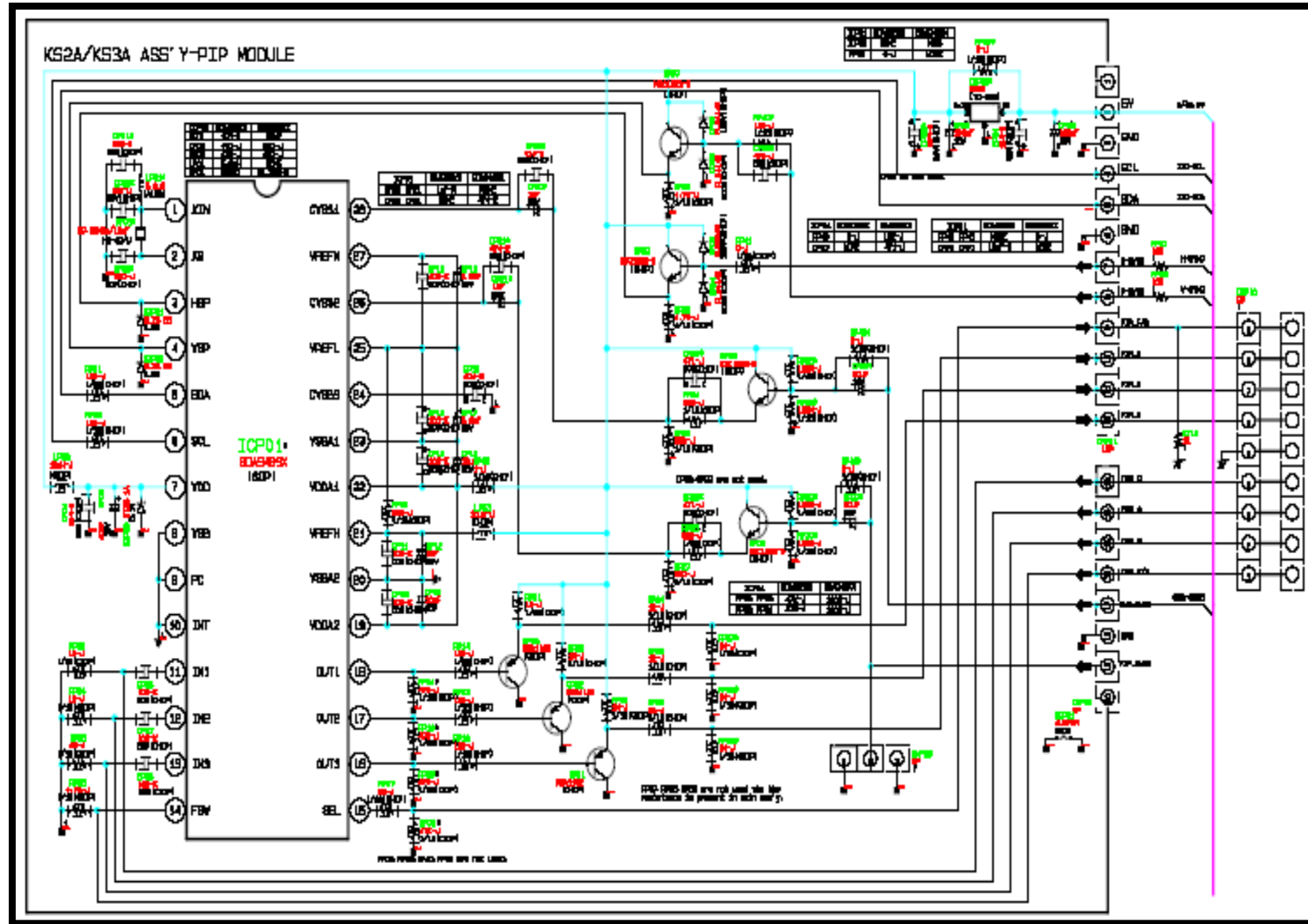
Spot Killer

※ When Picture and Master Power Off, Protection Circuitry of CRT Spot



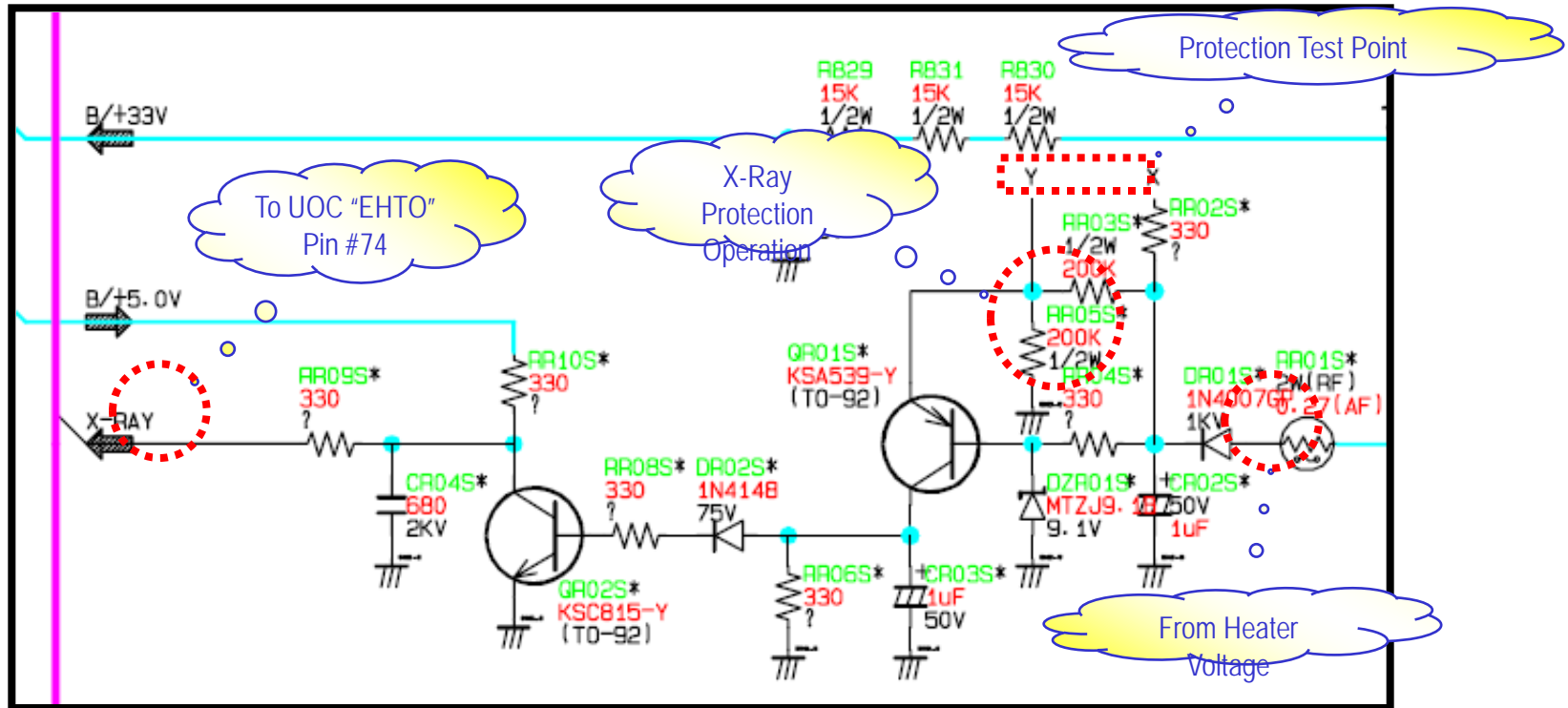
Picture In Picture

✖ Assy Sub PIP

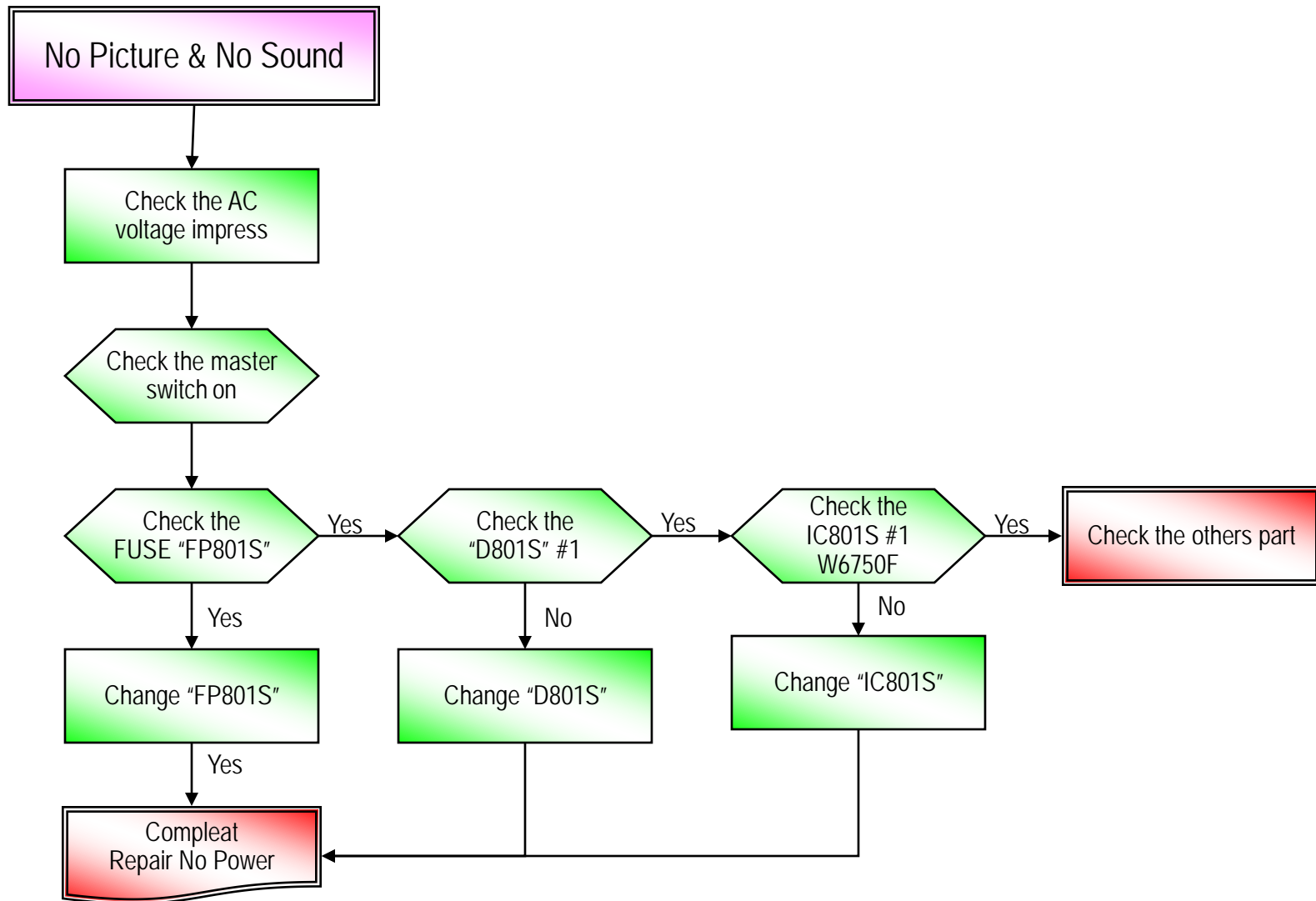


X-Ray Protection

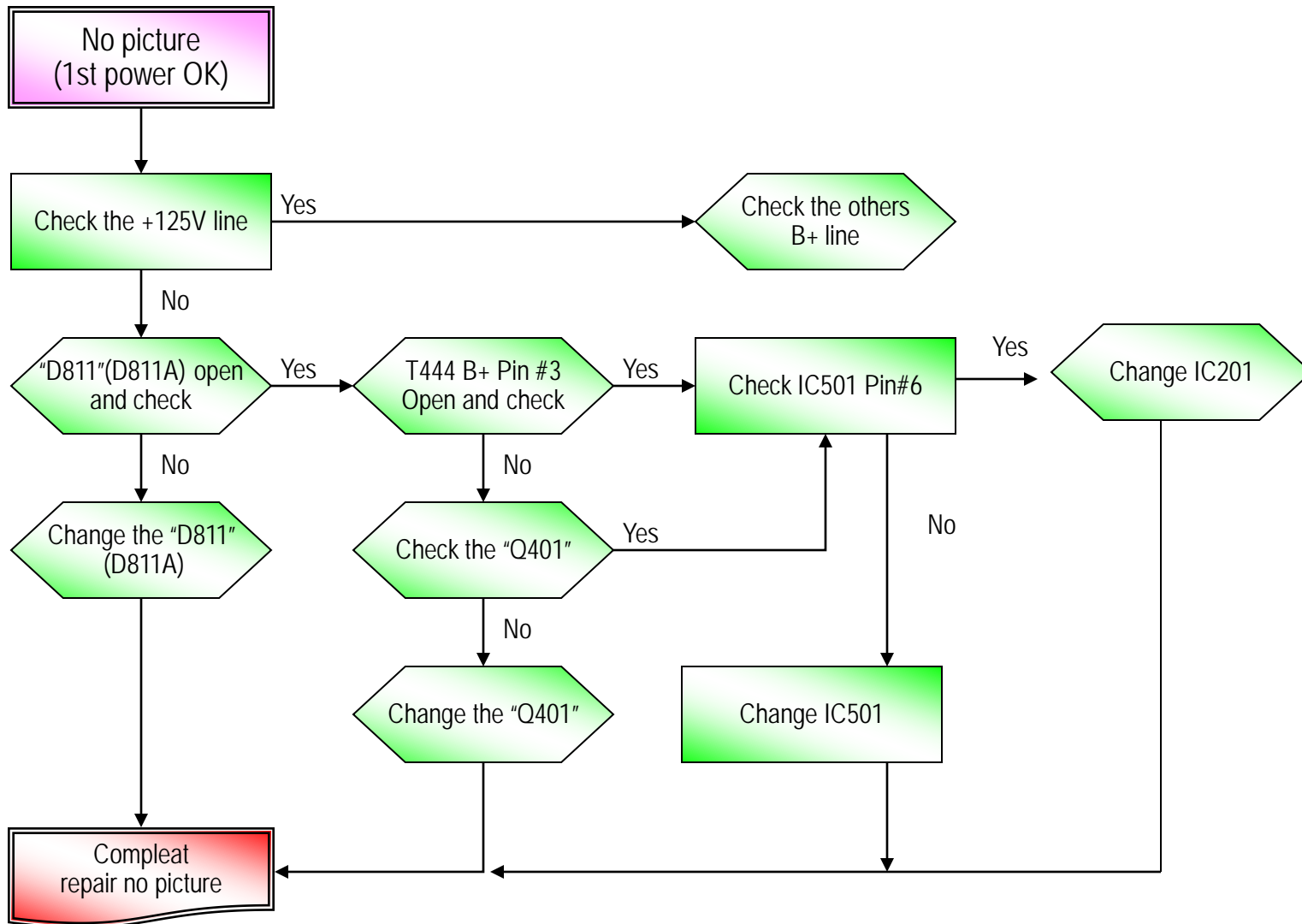
※ The change of Heater Voltage in accordance with the change of High Voltage



No Power(1st Power)



No Picture(2nd Power)



No Sound

